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NPS-SCAT: SYSTEMS ENGINEERING AND PAYLOAD SUBSYSTEM DESIGN, INTEGRATION, AND TESTING OF NPS' FIRST CUBESAT

by

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June 2010

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NPS-SCAT: SYSTEMS ENGINEERING AND PAYLOAD SUBSYSTEM DESIGN, INTEGRATION, AND TESTING OF NPS' FIRST CUBESAT

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ABSTRACT

The Naval Postgraduate School's first CubeSat, the NPS Solar Cell Array Tester (NPS-SCAT), demonstrates the capability of the CubeSat form factor as a technology test bed by implementing a single experiment—a solar cell tester. The need to validate solar cell performance on orbit, in the harsh space environment, is recurring with the continued development of advanced, untested solar cells. By using a relatively inexpensive platform, the CubeSat, such solar cells can be tested and the risk for larger satellites mitigated with this experiment. This thesis discusses the design and construction process of the solar cell array tester payload along with its integration with the remaining satellite subsystems (command and data handling subsystem, communications subsystem, and electrical power subsystem) including the problems encountered along the way and the chosen solutions. In addition, the systems engineering and testing procedures developed for and conducted on the satellite engineering design unit will be described in detail.

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LIST OF ABBREVIATIONS AND ACRONYMS

/SS	Slave Select (active low)
1U	One Unit CubeSat
2U	Two Unit CubeSat
3D	Three Dimensional
A/R	Anti-reflective
AAUsat	Aalborg University Satellite
ABS	Acrylonitrile Butadiene Styrene
ACS	Attitude Control Subsystem
ADAMASat	Antenna Deployment and Mono-filament Actuator Satellite
ADC	Analog to Digital Converter
ADCS	Attitude Determination and Control Subsystem
AM	Air Mass
ANSI	American National Standards Institute
APD	Avalanche Photo Diode
ARC	Ames Research Center
ASTM	American Society for Testing and Materials
ATJ	Advanced Triple Junction
AU	Astronomical Unit
AWG	American Wire Gauge
BCR	Battery Charge Regulator
C&DH	Command and Data Handler
CAD	Computer Aided Design
Cal Poly	California Polytechnic State University
CanX	Canadian Advanced Nanospace Experiment
CDS	CubeSat Design Specification
CERTO	Coherent Electromagnetic Radio Tomography
CFTP	Configurable Fault Tolerant Processor
CIC	Cell-Interconnect-Coverglass

COTS	Commercial-Off-The-Shelf
CONOPS	Concept of Operations
CPT	Comprehensive Performance Test
CSK	CubeSat Kit
CSTB1	CubeSat TestBed 1
CUTE	Cubical Titech Engineering Satellite
DAC	Digital to Analog Converter
DIP	Dual In-Line Package
DoD	Department of Defense
DPDT	Dual Pole Dual Throw
EDU	Engineering Design Unit
EELV	Evolved Expendable Launch Vehicle
EMI	Electromagnetic Interference
EPS	Electrical Power Subsystem
EPS1	First Revision of Clyde Space EPS
EPS2	Second Revision of Clyde Space EPS
ESA	European Space Agency
ESP	Experimental Solar Panel
ESPA	EELV Secondary Payload Adapter
FHSS	Frequency Hopping Spread Spectrum
GEO	Geosynchronous Equatorial Orbit
GEVS	General Environment Verification Specification
GOES	Geostationary Operational Environmental Satellite
GPIO	General Purpose Input Output
GSEAS	Graduate School of Engineering and Applied Science
I^2C	Inter-Integrated Circuit
I-DEAS	Integrated Design and Engineering Analysis Software
IC	Integrated Circuit
I_{SC}	Short-Circuit Current
ISIS	Innovative Solutions In Space

ISS	International Space Station
ITJ	Improved Triple Junction
JAXA	Japan Aerospace Exploration Agency
kB	kilobyte
LEO	Low Earth Orbit
LDO	Low Drop Out
LV	Launch Vehicle
MAE	Mechanical and Astronautical Engineering
MARECS	Maritime European Communication Satellite
MAST	Multi-Application Survivable Tether
MEFL	Maximum Expected Flight Level
MISO	Master Input, Slave Output
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSI	Master Output, Slave Input
MPPT	Maximum Power Point Tracker
NASA	National Aerospace and Space Administration
NC	Not Connected
NPS	Naval Postgraduate School
NPSAT1	NPS Spacecraft Architecture and Technology Demonstration Satellite
NPSCuL	NPS CubeSat Launcher
Op-Amp	Operational Amplifier
P-POD	Poly-Picosatellite Orbital Deployer
PANSAT	Petite Amateur Navy Satellite
PARADIGM	Platform for Autonomous Rendezvous And Docking with Innovative GN&C Methods
PCB	Printed Circuit Board
P_{MAX}	Maximum Power Point
PRESat	PharmaSat Risk Evaluation Satellite
PSLV	Polar Satellite Launch Vehicle
PSSC	Pico-Satellite Solar Cell Testbed

PV	Photovoltaic
RAFT	Radar Fence Transponder
RAM	Read-And-write Memory
RBF	Remove-Before-Flight
RTC	Real Time Clock
RTOS	Real-Time Operating System
SCAT	Solar Cell Array Tester
SCK	Serial Clock
SCL	Serial Clock
SD	Secure Digital
SDA	Serial Data
SEEDS	Space Engineering Education Satellite
SEPIC	Single Ended Primary Inductor Converter
SERB	Space Experiments Review Board
SMS	Solar Cell Measurement System
SNAP	Surrey Nanosatellite Applications Platform
SOCEM	Sub-Orbital CubeSat Experimental Mission
SOIC	Small Outline Integrated Circuit
SOT	Small Outline Transistor
SpaceX	Space Exploration Technologies Corporation
SPI	Serial Peripheral Interface
SPL	Single Picosatellite Launcher
SSAG	Space Systems Academic Group
SSDL	Space Systems Development Laboratory
SSETI	Student Space Exploration and Technology Initiative
SSPL	Space Shuttle Payload Launcher
SSTL	Surrey Satellite Technology Limited
STK	Satellite Tool Kit
STP	Space Test Program
STS	Space Transportation System

T-POD	Tokyo Picosatellite Orbital Deployer
TASC	Triangular Advanced Solar Cell
TCS	Thermal Control Subsystem
TINYSCOPE	Tactical Imaging Nanosatellite Yielding Small Cost Operations for Persistent Earth Coverage
TISARP	Tiny Spacecraft Assembly, Reconfiguration and Proximity-Operations
TSSOP	Thin Shrink Small Outline Package
TTL	Transistor-Transistor Logic
TVAC	Thermal Vacuum Chamber
UHF	Ultra High Frequency
USB	Universal Serial Bus
USNA	United States Naval Academy
UTJ	Ultra Triple Junction
μC	Micro-Controller
V_{OC}	Open-Circuit Voltage
VBAT	Battery Voltage
XPOD	eXperimental Push Out Deployer
XI	X-factor Investigator

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I. INTRODUCTION

A. CUBESAT DEFINITION AND HISTORY

The CubeSat form factor for very small satellites (also known as picosatellites) was developed in 1999 by Professor Bob Twiggs of Stanford University and Professor Jordi Puig-Suari of California Polytechnic State University (Cal Poly). The goal of the CubeSat idea was to promote education in space engineering, reduce the time and cost of satellite development, and enable more access to space while maintaining a standardization that would help accomplish these goals. Defined initially as a 10 cm cube with a mass of no more than 1 kg, now upped to 1.33 kg, the CubeSat form factor has provided quick and relatively inexpensive payloads to be developed by "over 100 universities, high schools, and private firms" [1].

When it was first established, the CubeSat concept was initially popular with universities interested in its value to a satellite design program with the possibility of actually flying the product in a reasonable timeframe. As time went by, more and more universities and private and government organizations began to see the value offered by the small, yet capable CubeSat. Despite its size, the CubeSat has, at the very least, the ability to educate future space professionals, mitigate risk for larger satellites, and act as an experimental test bed. It may even prove to be an operational asset in the near future.

Several different CubeSat form factors have been brought into being from the original 10 cm size. Defined as a one unit, or U, the 10 cm-on-a-side cube can be stacked to form larger versions. These larger versions are defined by the number of units they contain; for example: two 10 cm cubes stacked represents a 2U CubeSat. The maximum number of CubeSat units that can be launched at this time is three, based upon the capacity of the Cal Poly-developed CubeSat launcher, the Poly-Picosatellite Orbital Deployer (P-POD), seen in Figure 1. As long as the CubeSat being developed is within the parameters defined by the CubeSat Design Specification (CDS), it will be able to be

launched from a P-POD [1]. The P-POD is secured to a launch vehicle (LV), acts as the interface between the CubeSat and LV, and when commanded, will launch the CubeSats using a spring-loaded pusher plate [1].

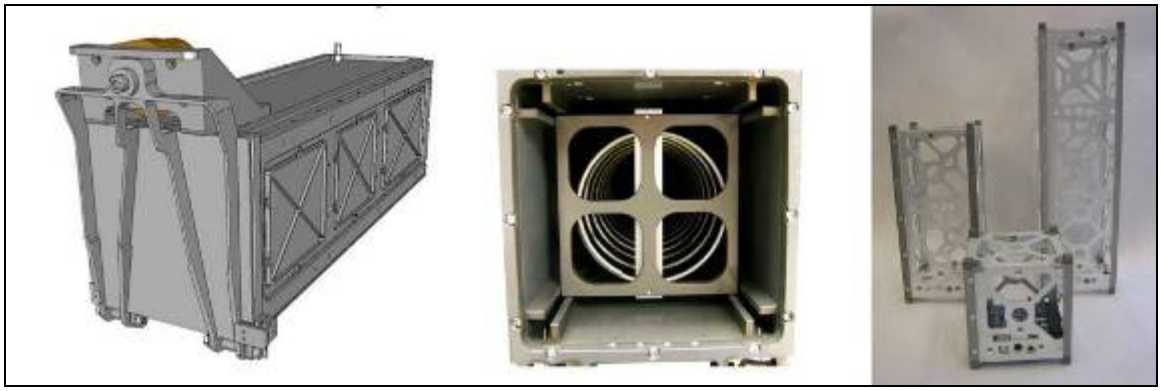

Figure 1 P-POD (From [1]) and CubeSat Structures (2U, 1U, 3U)

Several other organizations have designed and built their own launchers for CubeSats. The Japanese institutions of Tokyo University and Tokyo Institute of Technology developed the T-POD (Tokyo Picosatellite Orbital Deployer) which was first used on a Russian Eurockot in 2003 to deploy the XI-IV and CUTE-I CubeSats [2, 3]. This launcher is comparable to the P-POD in its operation by pushing out the CubeSats and has very similar dimensions, which meet the CubeSat Design Specification. The XPOD (eXperimental Push Out Deployer), created by the University of Toronto's Institute of Aerospace Studies Space Flight Laboratory to deploy its own satellites, was first used to launch CanX-2 from a Polar Satellite Launch Vehicle (PSLV) in 2008 [4]. The XPOD supports multiple form factors, some exceeding the CDS dimensions but keeping a general cube-shape [5]. The Single Picosatellite Launcher (SPL) was developed by the German company Astro-und Feinwerktechnik Adlershof GmbH and launches a single CubeSat. It adheres to the CDS but provides "additional space for attached external components on the bottom" [6]. This design was successfully flight-proven in 2009 when the PSLV C14 was launched with multiple CubeSats onboard [7]. Within the United States, NASA Ames Research Center, in collaboration with Cal Poly, has begun development of a launcher capable of launching a larger "satellite that is approximately equivalent to the size and mass of 6 CubeSats" [8].

B. CUBESATS — PAST AND PRESENT

As of this writing, there have been a total of 52 CubeSats integrated onto launch vehicles. Of these 52 satellites, only 34 were successfully injected into low earth orbit. The first CubeSats were launched on 30 June 2003 on a Russian Eurockot from Plesetsk, Russia [9]. This first bunch of six satellites were of mixed success, from the still operational Japanese-designed CUTE-I, to the highly successful United States' QuakeSat, to the Canadian CanX-1, which was never successfully contacted by a ground station. These first CubeSats were primarily research projects with the goal of miniaturizing experiments into a proof-of-concept design. The second group of CubeSats was launched on 27 October 2005 onboard a Kosmos-3M launch vehicle from the Russian Plesetsk Cosmodrome launch site. These three CubeSats were developed by several different European countries to form the student-designed project SSETI (Student Space Exploration and Technology Initiative) Express. The primary objective of these satellites was to develop a European workforce in the fields of space technology and science with hands-on spacecraft design experience [10].

The single Japanese 2U CubeSat, CUTE 1.7 + APD, was launched on 22 February 2006 as a subpayload of a JAXA M-V-8 rocket from the Uchinoura Space Center in Japan [11]. On 26 July 2006, a launch of fourteen CubeSats was attempted onboard the Russian Dnepr-1 rocket, a former ballistic missile converted to carry payloads into orbit. The launch vehicle, the seventh for the Dnepr-1 rocket, failed to reach orbit due to a premature separation of the first stage, causing the complete loss of all payloads onboard [12]. This was the largest CubeSat launch attempt to date with satellites developed by Japan, Norway, South Korea, and the United States. The large number of space vehicles lost made this launch failure a tragedy within the CubeSat community. NASA Ames Research Center developed and launched the 3U GeneSat-1 CubeSat on 16 December 2006 from Wallops Island, Virginia on a Minotaur 1 launch vehicle [13]. This nanosatellite was used to provide "life support and nutrient delivery" for E. coli bacteria and analyze its growth in the space environment [13]. With P-PODs attached to another Dnepr-1 rocket, the next batch of seven CubeSats was successfully orbited on 17 April 2007 from Baikonur Cosmodrome in Kazakhstan. Mostly from the

United States, these CubeSats were primarily replacement vehicles for those lost on the 2006 Dnepr-1 launch failure including the Aerospace Corporation's AeroCube-2, and Cal Poly's CP3 and CP4 [14]. Boeing also had their CubeSat TestBed 1 (CSTB1) onboard the launch, indicating larger aerospace corporations have become more than just interested in the CubeSat concept.

The first half of 2008 brought a launch of replacement and revised CubeSats for those lost on the 2006 Dnepr-1 launch failure. On 28 April 2008, a PSLV carrying six CubeSats was launched from Satish Dhawan Space Centre in India. These satellites had newly developed experiments or were improved versions of the first CubeSats launched in 2003 (AAUsat-2, CanX-2, CUTE 1.7 + APD II). One was a replacement for the Dnepr-1 failure (SEEDS) [9]. For the third flight of the Space Exploration Technologies Corporation (SpaceX) developed Falcon 1 rocket, NASA Ames Research Center (ARC) was able to secure a launch for their two 3U CubeSats, PRESat (PharmaSat Risk Evaluation Satellite) and NanoSail-D. This launch on 02 August 2008 from Omelek Island in the Kwajalein Atoll, however, ended in failure due to a problem with the second stage separation [15]. NASA ARC was able to successfully get the PharmaSat nanosatellite into orbit on 19 May 2009 onboard a Minotaur-1 launched from Wallops Island. PharmaSat's mission was to conduct biological tests on yeast to determine how quickly it adapts in space [16]. This launch vehicle also carried three more CubeSats, AeroCube-3, CP6, and HawkSat-I, into orbit. The next launch included two satellites developed by universities within the United States. Not technically CubeSats, these nanosatellites were slightly larger than the 10 cm specification, measuring 5 in (12.7 cm) on a side. Texas A&M's AggieSat2 and University of Texas' BEVO1 were deployed from the space shuttle Endeavor (STS-127) on 30 July 2009 from the Space Shuttle Payload Launcher (SSPL) located in the orbiter's cargo bay [17]. A follow-on CubeSat launch occurred on 23 September 2009 from a PSLV-C14, launched from the Indian Satish Dhawan Space Centre. These four satellites were developed by multiple nations: BEESAT was developed by the Technical University of Berlin; ITUpSAT1 was developed by Istanbul Technical University; SwissCube was built by the Swiss

Polytechnic School of Lausanne; and UWE-2 was created by the German University of Würzburg [9]. Data from this group of satellites has been down linked successfully.

The most recent pair of CubeSats to be launched, on 27 March 2010, were onboard a NASA suborbital Terrier-Improved Malemute sounding rocket from Wallops Island. The two satellites were ADAMASat (Antenna Deployment and Mono-filament Actuator Satellite) from the University of Kentucky and a Cal Poly CubeSat attitude determination testbed. Together, these two satellites comprised the Sub-Orbital CubeSat Experimental Mission (SOCEM), which attempted to demonstrate the sounding rocket as a platform for fast access to space [18]. The satellites re-entered the atmosphere within several minutes of ejection from the sounding rocket after successfully transmitting data to their respective ground stations.

The complete listing of the CubeSats launched to date can be seen in Table 1. It is organized by date of launch.

Table 1 List of CubeSats Launched

2003	2005	2006	2007	2008	2009	2010
30 June	**27 October**	**22 February**	**17 April**	**28 April**	**19 May**	**27 Mar**
AAU CubeSat	NCube2	CUTE 1.7 + APD	AeroCube-2	AAUsat-2†	AeroCube-3	ADAMASat
CanX-1	UWE-1	**26 July**	CAPE-1	CanX-2	CP6	Poly-Sat testbed
CUTE-I†	XI-V†	AeroCube-1*	CP3†	Compass One†	HawkSat-I	
DTUsat-1		CP1*	CP4†	CUTE 1.7 + APD II†	PharmaSat-1	
QuakeSat-1		CP2*	CSTB 1†	Delfi-C3†	**30 July**	
XI-IV†		HAUSAT 1*	Libertad-1	SEEDS (2)†	AggieSat2	
		ICE Cube 1*	MAST†	**02 August**	BEVO1	
		ICE Cube 2*		PRESat*	**23 September**	
		ION*		NanoSail-D*	BEESAT†	
		KUTEsat*			ITUpSAT1†	
		Mea Huaka*			SwissCube†	
		MEROPE*			UWE-2†	
		NCube1*				
		RINCON 1*				
		Sacred*				
		SEEDS*				
		16 December				
		GeneSat-1†				

†Indicates satellite still active

*Indicates launch vehicle failure

C. NPS SMALL SATELLITE DESIGN PROGRAM

The Space Systems Academic Group (SSAG) at the Naval Postgraduate School (NPS) was created in 1982 to develop a curriculum in support of a cadre of military officers with space systems experience [19]. In addition to two graduate curriculums, Space Systems Operations and Space Systems Engineering, the SSAG also has a Small Satellite Design Program focused on developing small satellites for graduate-level research, focusing on giving military officers hands-on experience in the satellite design cycle. The designation of "small" satellite can be broken down further into several classes based on the mass. A listing of the different classes of small satellites is shown in Table 2.

Table 2 Small Satellite Classification by Mass (From [20])

Spacecraft Class	Mass Range
Microsatellite	10 - 100 kg
Nanosatellite	1 - 10 kg
Picosatellite	0.1 - 1 kg
Femtosatellite	0.01 - 0.1 kg

1. PANSAT

The first satellite to be fully designed, built, and launched by the NPS SSAG was PANSAT (Petite Amateur Navy Satellite). PANSAT was designed to be a tumbling communications satellite, providing "store-and-forward communications using spread-spectrum techniques in the UHF amateur frequency bands" [19]. It was launched from the space shuttle Discovery on 29 October 1998, as shown in Figure 2, operated for almost four years, and is still in orbit today.

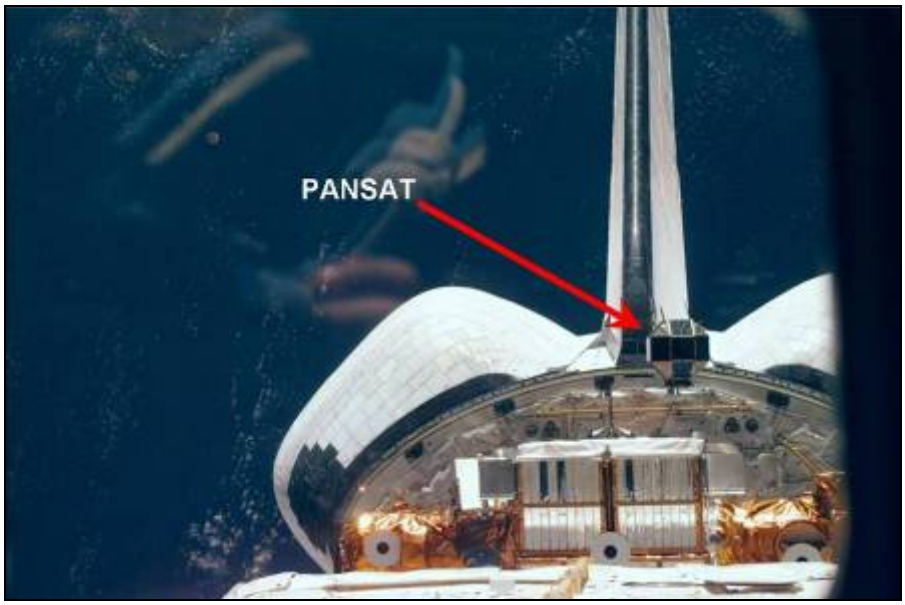

Figure 2 PANSAT Deployment (After [19])

2. NPSAT1

The next satellite to be designed at NPS was NPSAT1 (Naval Postgraduate School Spacecraft Architecture and Demonstration Satellite), shown in Figure 3. Currently still in development, this satellite "will serve as a test bed for small satellite technology as well as an experiment platform" [19]. NPSAT1 is a three-axis stabilized satellite that contains several payloads including a configurable fault tolerant processor (CFTP), solar cell measurement system (SMS), a commercial-off-the-shelf (COTS) camera, and two Naval Research Laboratory experiments: a coherent electromagnetic radio tomography (CERTO) beacon and Langmuir probe. It is configured to be launched from Atlas V Evolved Expendable Launch Vehicle (EELV) Secondary Payload Adapter (ESPA).

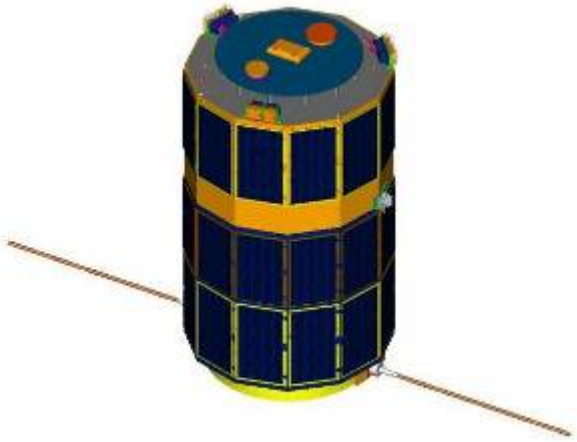

Figure 3 NPSAT1 (From [21])

3. NPSCuL

As mentioned previously, the majority of the CubeSats have launched overseas using primarily Russian and Indian launch facilities. The NPS CubeSat Launcher (NPSCuL) program attempts to bring the CubeSat launch capability to the United States, offering a minimum of 24U volume capacity in a single launch. The concept is very simple, integrating several P-PODs together into a single structure, shown in Figure 4. Two different versions have been designed: NPSCuL, with 50U launch capacity, and NPSCuL-Lite, with 24U launch capacity. The structure is then integrated onto the launch vehicle using the ESPA ring (Figure 5).

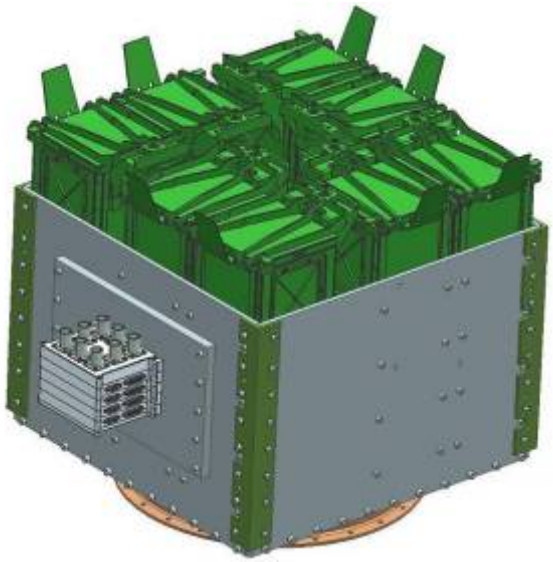

Figure 4 NPSCuL-Lite integrated with P-PODs (From [22])

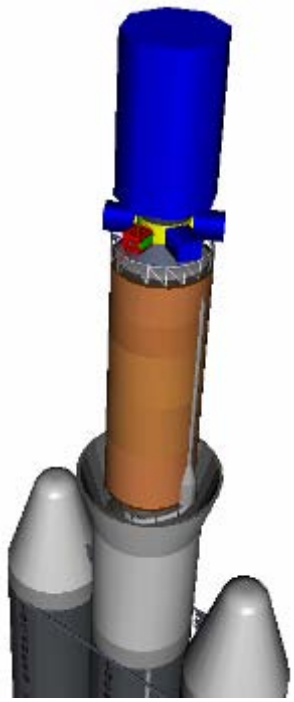

Figure 5 NPSCuL on Atlas V ESPA Ring (From [23])

4. TINYSCOPE

Another small satellite in development within NPS' Nanosatellite Advanced Concepts Laboratory is TINYSCOPE. This project, also known as Tactical Imaging Nanosatellite Yielding Small Cost Operations for Persistent Earth Coverage, is a 6U nanosatellite and has a primary objective of delivering tactical imagery within a timeframe to be practically useful to the war fighter on the ground (Figure 6). A concept for a TINYSCOPE constellation is also in development to provide the operational benefit of worldwide coverage at any time.

Figure 6 TINYSCOPE CubeSat Concept (From [24])

5. NPS-SCAT

The first CubeSat to be designed, built, and tested at NPS is the Naval Postgraduate School Solar Cell Array Tester (NPS-SCAT). NPS-SCAT is a 1U CubeSat with a primary payload to test solar cells and measure their degradation over time due to interactions with the space environment. This satellite, which will be described in greater detail in the remainder of this thesis, is based on the SMS experiment from NPSAT1.

D. THESIS OBJECTIVE

The objective of this thesis is to advance the design of the solar cell array tester payload of the NPS-SCAT CubeSat. With solar cells being the main source of power for satellites, it is important to know how they operate and degrade when exposed to the

harsh environment of low earth orbit. The design of the NPS-SCAT payload will require an understanding of how to measure solar cell characteristics, an innovative circuit board design and layout to fit within the CubeSat form factor, and the development of additional circuit boards to serve as solar panels. Once designed, the payload needs to be integrated with the remaining subsystems, which rely primarily on commercial-off-the-shelf components. This thesis describes all facets of this process from design and construction to final system and subsystem testing.

To gain an understanding of the thermal environment in which the satellite will be exposed, a model of the satellite using a single thermal node will be developed. The data from this model will be used to determine whether the components chosen for the payload and remaining subsystems will withstand the space environment. In addition to the payload development and thermal model, the satellite engineering design unit will undergo a thermal vacuum test, which will be described, including the test plan that was developed and the results gathered. The outcome of this work can be used to construct and integrate the NPS-SCAT flight unit.

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II. OVERVIEW OF NPS-SCAT MISSION AND PROGRAM OBJECTIVES

A. SPACECRAFT MALFUNCTIONS DUE TO SOLAR CELL DEGRADATION

Solar cells are the primary power-producing agents used onboard spacecraft and have been since the start of the space age in the 1960s. Since man-made satellites have been orbiting the earth, there have been numerous failures caused by interactions with the space environment. Solar cell failure can be linked as the cause of several satellite malfunctions or reduced lifetime on orbit.

The space environment contains many elements that cause harm to spacecraft solar arrays. The environment includes "both naturally occurring phenomena such as atomic oxygen and radiation and man-made factors such as orbiting debris" [25]. It can be shown that the interactions with solar and cosmic radiation produce the most damage to solar cells. For example, in March 1991 there was an intense solar flare released from the upper atmosphere of the sun. Several satellites in geosynchronous equatorial orbit (GEO) were severely affected including the Geostationary Operational Environmental Satellites (GOES) weather satellites units five and seven. "The GOES-7 power degradation translated to a decrease of 2 to 3 years in expected satellite lifetime" [25]. Another satellite that failed due to solar panel damage was MARECS-1, the Maritime European Communication Satellite. Several other solar events have occurred, damaging the solar panels of four Cluster II satellites and the Tempo 2 satellite, which is now designated DirecTV 6. Solar radiation trapped by the earth's magnetic field, known as the Van Allen belts, is also a known culprit for causing solar cell failure; for example, the Japanese ETS-6 (Engineering Test Satellite) solar arrays were "quickly eroded" when it was accidently placed into the wrong orbit [25].

The mission of the NPS-SCAT satellite addresses the above problems by providing a quantitative measurement of how the space environment degrades solar cells over time. Future iterations of this experiment offer untested solar cells the opportunity

to be flown in space and validate their expected performance. Satellite manufacturers can reduce their risk with the empirical knowledge of a solar cell's expected lifetime when exposed to real-life threats of the space environment.

B. SOLAR CELL THEORY

To properly understand the full functionality of the NPS-SCAT payload, the mechanics and operation of a solar cell need to be explained.

1. Basics

The solar cell is a device that uses the photovoltaic (PV) effect to produce electrical power. Discovered in 1839, the PV effect "is the direct conversion of light into electricity at the atomic level" [26]. When photons, energetic particles of light, interact with certain materials, such as the semiconductor silicon, energy is transferred from the photon to the valence electrons of the material. If the energy is "equal to or greater than the band gap of the cell material," an electron will be freed to be used by an electric circuit [26]. Different energies of photons, correlating to different wavelengths of light, will be absorbed by the different types of cell material, as seen in the two plots of Figure 7. Quantum efficiency is the measure of the percentage of photons that are absorbed by a certain substance; in this case the different solar cell materials [27]. The location of the interaction between the photons and a single material type is known as a junction. To produce a highly efficient cell, multiple material types, each with different band gap energies, are placed together to form a layer of multiple junctions that is able to absorb a wide range of wavelengths of light.

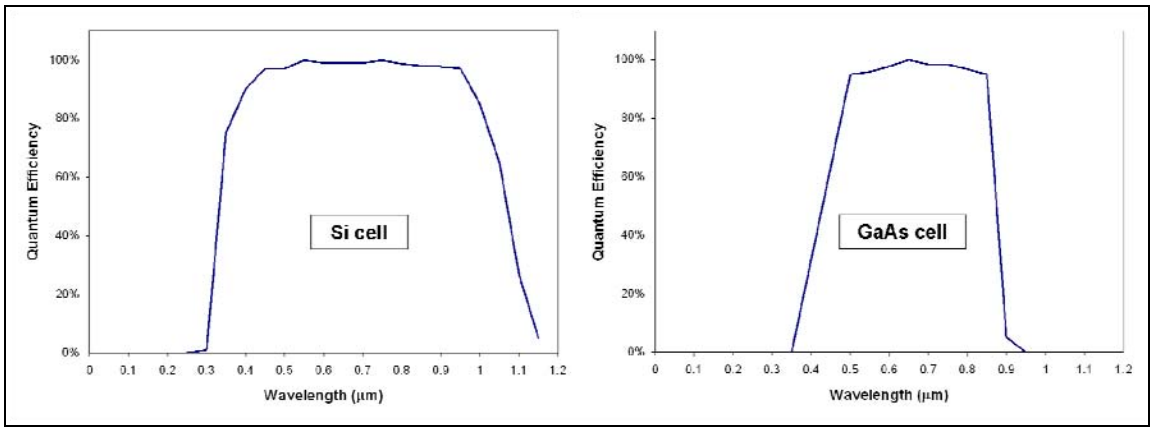

Figure 7 Quantum Efficiency vs. Wavelength for Different Solar Cells (After [28])

The most common solar cells are single junction constructed of silicon (Si). For many years, this was the standard for spaceflight and now these types of solar cells are being utilized for terrestrial applications. Through advancements in technology brought about by the space industry, modern space-grade solar cells are now typically triple junction and manufactured using materials such as gallium arsenide (GaAs), gallium indium phosphide (GaInP2), and germanium (Ge). There are slight trade-offs when selecting either type, as "gallium arsenide solar cells produce twice as much power as silicon and are more durable, while silicon solar cells weigh less and conduct heat better" [29]. Space-rated solar cells are produced with a layer of anti-reflective (A/R) coating on top to minimize the amount of light that is reflected, thereby maximizing the light available to be converted into electrical energy [30]. A visual diagram comparing single junction and triple junction solar cells is shown in Figure 8.

The basic single junction solar cell can be modeled as the equivalent circuit shown in Figure 9. The circuit shows the current density, J_{PH}, produced by the solar cell when it is illuminated. There is a loss to this current in the back flow of electrons through the diode, simulating the physical junction between materials. For a multiple junction solar cell, there would be another diode added in series for each additional junction. The resistors in the circuit represent external factors that add to the drop in solar cell efficiency. For an ideal cell, the shunt resistance, R_{SH}, is infinite and the series

resistance, R_{SR}, is zero. However, due to imperfections in the manufacturing process, representative of R_{SH}, and soldering connections, modeled by R_{SR}, this is not the case for a real solar cell and, therefore, the actual efficiency is less than ideal [31].

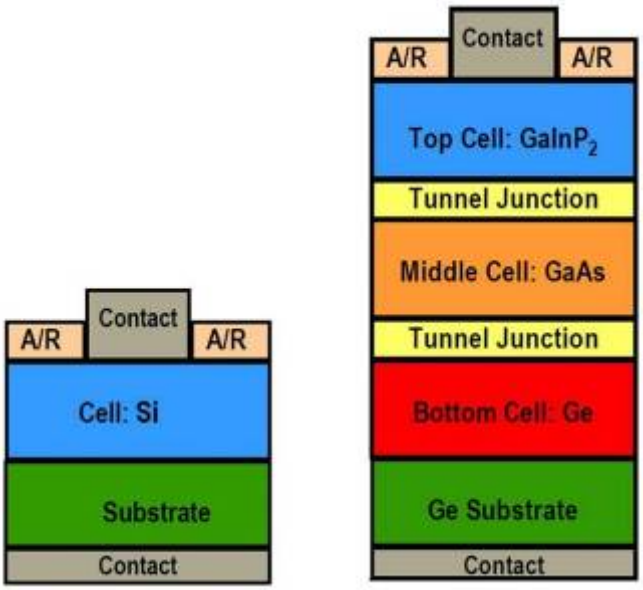

Figure 8 Silicon Single Junction and Improved Triple Junction Solar Cells (After [32])

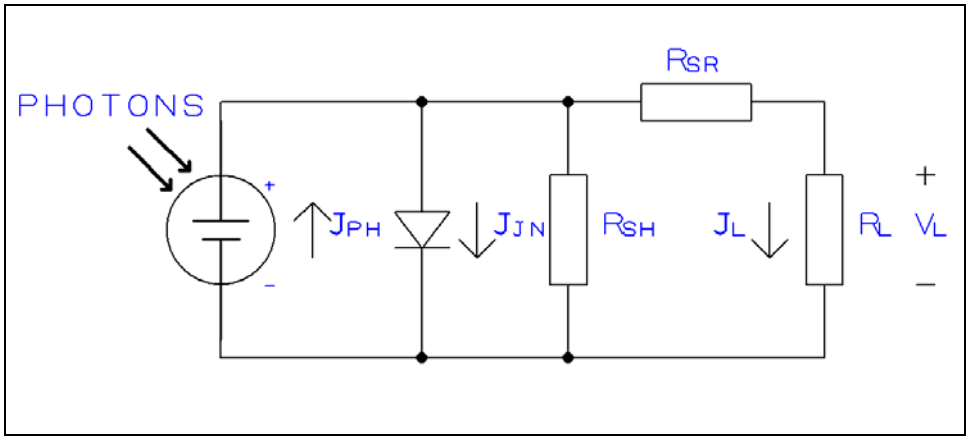

Figure 9 Solar Cell Equivalent Circuit (After [31])

2. Factors Affecting Performance

Several factors affect the output of a solar cell and must be taken into account when determining solar cell performance, either for characterization purposes or operational need. These include light intensity, light incidence angle, temperature, physical area of the solar cell, and any damage that may have been experienced by the solar cell.

a. Light Intensity

Light intensity, also known as spectral irradiance, is a measure of the "energy per unit wavelength" of electromagnetic radiation [27]. Because the sun is the primary source of light, which itself is part of the electromagnetic spectrum, it is intuitive that there exists a relationship between the sun's intensity and solar cell power output. The solar cell output is directly proportional to light intensity; when the light intensity is increased, so is the solar cell output [28, 33]. Throughout the year, as the Earth orbits the Sun, "the intensity of the sunlight reaching Earth varies approximately ±3.5%" due to the nature of the elliptical orbit [34]. As a black body radiator, the sun emits an irradiance, or solar flux, that has been designated to be 1366.1 W/m2 by the American Society for Testing and Materials (ASTM) when measured from the Earth's average distance to the Sun of one astronomical unit (AU). One also must factor in the air mass (AM) value when determining solar flux on earth. The ASTM has also developed a standard for air mass references. Air mass refers to the amount of atmosphere the sunlight must pass through before reaching the solar cell; as sunlight passes through the atmosphere, it is scattered and absorbed which reduces the overall flux. When the sun is directly overhead at the observer's zenith, this is known as AM1. Air mass can be calculated using the angle between the observer's zenith and the sun, shown in Equation 2-1 [35]. This relationship can be visually seen in Figure 10. The air mass value in space, where there is no atmosphere, is AM0.

$$AM = \frac{1}{\cos\theta_{zenith}} \tag{2-1}$$

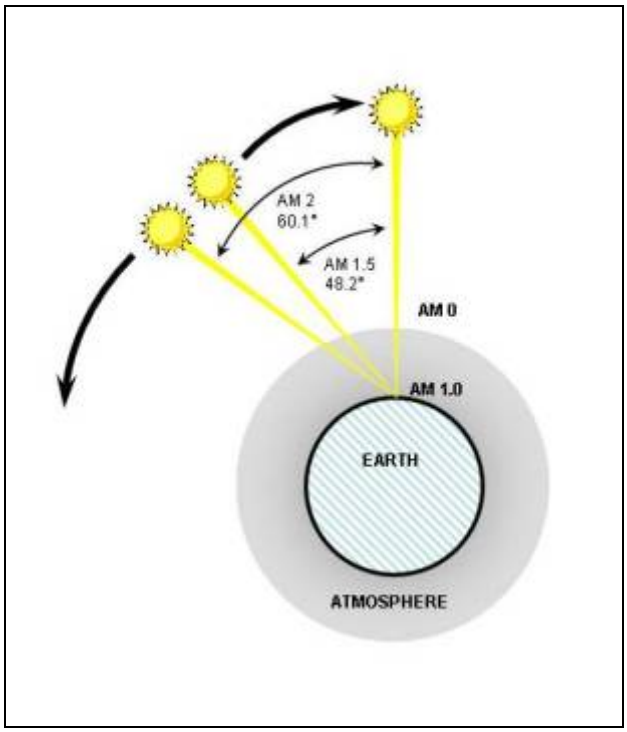

Figure 10 Air Mass Number Calculation (From [36])

b. Light Incidence Angle

The light incidence angle is the "angle between the incident light ray and the normal to the surface" as shown in Figure 11 [36]. The incident light ray is represented in the figure by the sun vector. This angle is measured from the surface normal to the incidence light ray; for example, when the incidence light ray is directly overhead, coinciding with the surface normal, the angle has a value of zero. The power output of a solar cell is proportional to the cosine of the light incidence angle. As the angle increases, the current output of the solar cell decreases; the maximum output is produced when the light incidence angle is zero. This response has been shown to follow Lambert's cosine law and is reproduced as Equation 2-2, where I_{SC} is defined as the calculated short-circuit current, *I0* is the short-circuit current when the incident angle is zero, and θ_i is the incident angle [37].

$$I_{SC} = I_0 \cos\theta_i \qquad (2\text{-}2)$$

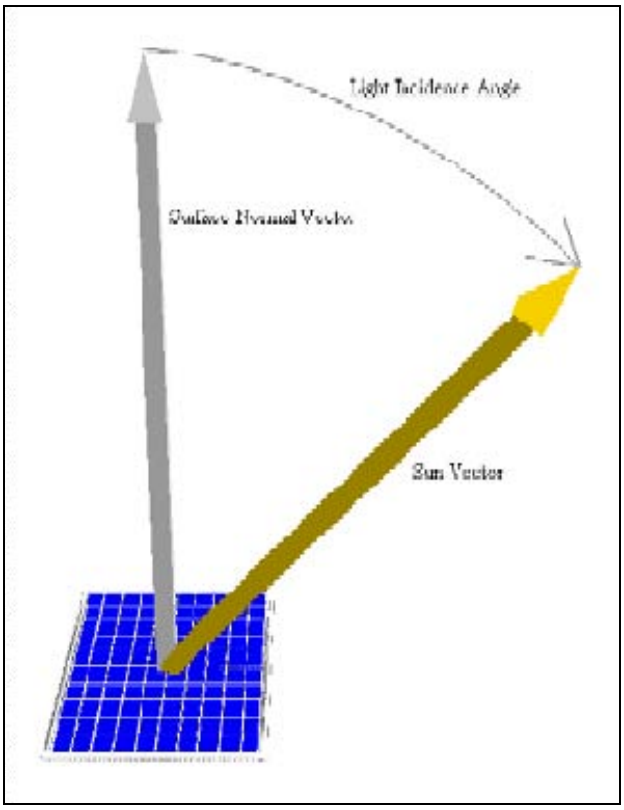

Figure 11 Light Incidence Angle Definition

c. Temperature

The temperature of the solar cell also has an effect on the produced output. "An increase in the cell operating temperature causes a slight increase in the cell short-circuit current and a significant decrease in cell voltage" [33]. A plot of the solar cell current and voltage, which is known as an I-V curve and is used to characterize solar cells, at different cell temperatures is shown in Figure 12.

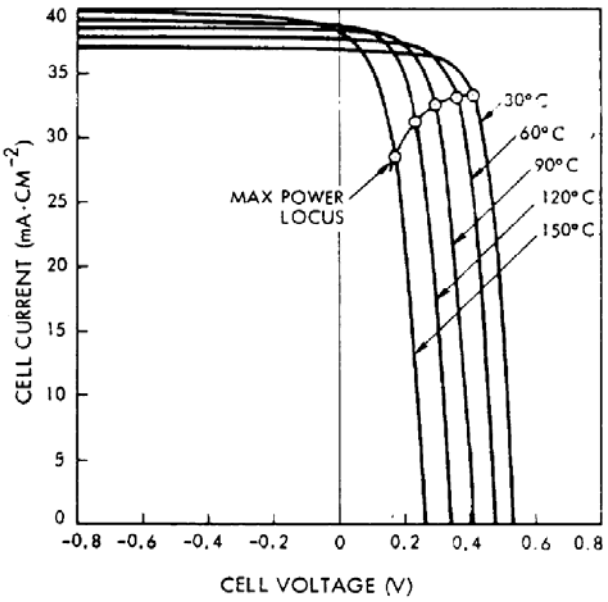

Figure 12 Effects of Temperature on Solar Cell Performance (From [33])

d. Area

Solar cells are manufactured such that each cell produces a relatively constant voltage output. This voltage level is set by the type of material used. The current, however, is dependent on the physical size of the solar cell. As the area of the solar cell increases, the output current also increases linearly [33]. Conversely, if a solar cell were to be diced into a smaller section, it would produce the same voltage but with reduced current. Most solar cell manufacturers give output current specifications of their solar cells with values normalized to the cell area, also known as current density.

e. Damage

The primary source of damage that occurs to solar cells is caused by ionizing radiation. Radiation, in the form of "high velocity, massive particles (electrons, protons, neutrons, or ions)" interacts on the atomic level within the affected solar cell to cause damage [31]. Atomic collisions between the radiation particles and the cell material cause disruptions in the cell's structure, which produces inherent inefficiencies and reduced output. Another particle that predominantly makes up the atmosphere from about 200 km to 600 km in altitude is atomic oxygen; "[t]his form of oxygen can react

with thin organic films" and degrade performance [38]. Some solar cells are protected by a coverglass that is used to protect the solar cell from degradation caused by atomic oxygen. This coverglass can, however, become clouded due to the ionizing effects of radiation; this reduces the amount of available light that the solar cell experiences. Other forms of damage can occur before launch due to mishandling, such as moisture and physical damage, and can be controlled with proper procedures.

C. NPS-SCAT OBJECTIVE

The primary objective of the NPS-SCAT satellite is to develop a space borne system that is capable of autonomously measuring the characteristics of several experimental solar cells to determine the rate of degradation. Secondary to this, but still critical to success, is the development of a standard CubeSat bus that is based primarily on commercial-off-the-shelf (COTS) components and will be used by future NPS experiments that require spaceflight. The use of the CubeSat form factor has given the satellite the flexibility and capability to be launched on any P-POD capable platform. Constant throughout the project's scope is the educational, hands-on experience available to the students and staff involved.

D. PAST WORK ON NPS-SCAT

1. Prototype

The development of NPS-SCAT began with the construction of a prototype unit by Alex Bein [39]. The initial prototype consisted of a Pumpkin CubeSat Kit that included a 1U Pumpkin Structure, Pumpkin Linear Power Supply with two lithium-ion cells (non-flight capable), an onboard Texas Instruments MSP430F1612 microcontroller, a Microhard MHX-2420 radio transceiver, and a custom-made solar cell measurement system (SMS) circuit. The solar cells chosen to provide power and to be tested by the prototype SMS circuit were Spectrolab Triangular Advanced Solar Cells (TASC). To measure the sun angle, a Sinclair Interplanetary SS-411 sun sensor was chosen due to its capability. The completed prototype unit is shown in Figure 13.

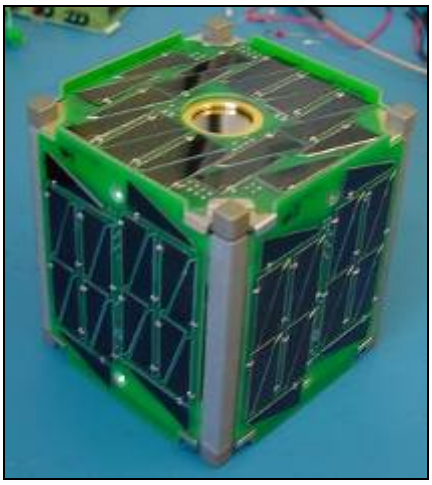

Figure 13 NPS-SCAT Prototype (From [39])

2. Engineering Design Unit

Upon completion of the prototype, this author began work on the engineering design unit (EDU), which refined and added more complexity to the prototype. The payload was redesigned, to be described in chapter three, the communications subsystem was updated to meet the power capabilities, and an electrical power subsystem (EPS) was selected which is spaceflight capable. Unless otherwise specified, documented, annotated, or referenced, the work described was completed by the author.

a. Communications Subsystem

The primary communications subsystem hardware initially chosen for the NPS-SCAT satellite was the Microhard MHX-2420 2.4 GHz radio transceiver [39]. This component is strictly COTS and was marketed by the Pumpkin Corporation to be fully compatible with the CubeSat Kit. After several unsuccessful attempts in using the MHX-2420 with the Clyde Space 1U EPS, a comprehensive test of the MHX-2420's power consumption was conducted by Matt Schroer [40]. This test revealed a transient power draw of approximately 13 W, which exceeded both the written specifications for the MHX-2420 and the capabilities of the EPS [40]. Due to this discovery, the MHX-2420 was deselected as the primary radio for NPS-SCAT and replaced by the MHX-2400, a slightly older but spaceflight-proven model, which has a transient power draw within the capability of the EPS [41].

In addition to the primary communications subsystem, a secondary communications subsystem was identified as desirable to provide communications redundancy and risk mitigation. Produced in the form of a beacon transmitter, this system is being developed in cooperation with Cal Poly's CubeSat program. Analysis for this system has been conducted based on initial estimates but, due to a lack of hardware, no physical testing has been carried out to date [40].

b. Electrical Power Subsystem

The Clyde Space 1U EPS was selected for use in the NPS-SCAT flight unit, replacing the Pumpkin non-flight Linear EPS. This power system is designed to be fully compatible with the CubeSat Kit and allows power produced by solar panels to be utilized for battery charging and spacecraft power usage. An initial analysis on the functionality of the Clyde Space 1U EPS1, the first revision of the Clyde Space 1U EPS, has been conducted by Lawrence Dorn, documenting the charge and regulator efficiencies [42]. In addition, a preliminary power budget was created based on the power consumption of the NPS-SCAT subsystems showing positive power margin by selecting appropriate duty cycles for the communications subsystem, typically the most power hungry subsystem [42].

3. SERB/STP Process

One route for a Department of Defense (DoD) designed experiment to be launched into space is for it to be vetted through the Space Experiments Review Board (SERB) process. Each experiment must go through two evaluations to be offered a flight opportunity: one with the respective service and, if successfully ranked, a second review at the DoD level. A SERB ranking is used to provide a general indication of the priority and likelihood for a space flight. The Space Test Program (STP) manages the SERB and arranges "flights of opportunity on domestic and foreign spacecraft" [43]. The STP reviews the SERB list and then selects appropriate experiments for available launch opportunities based upon their ranking. The NPS-SCAT experiment has been ranked by the Department of the Navy (DON) and DoD SERBs for both 2008 and 2009 and is thus eligible for an STP space flight opportunity (Table 3).

Table 3 NPS-SCAT SERB Rankings

Year	SERB	Rank
2008	DON	38/44
	DoD	58/62
2009	DON	19/24
	DoD	54/60

4. NPS-SCAT++

After the 2008 DoD SERB, the STP offered the NPS-SCAT experiment a possible launch opportunity onboard the Space Shuttle. The Space Shuttle has the ability to launch a small payload with a volume of five inches by five inches by ten inches (12.7 cm by 12.7 cm by 25.4 cm) from the Space Shuttle Payload Launcher (SSPL) 5510. The SSPL-5510 is located in the payload bay of the Space Shuttle and launches its payload in a similar manner as the P-POD, using a spring loaded pusher plate. However, the launch-able volume of the SSPL-5510 is slightly larger than the CubeSat form factor. In order for the NPS-SCAT CubeSat to be launched on this flight opportunity, either a complete redesign of the satellite must be done, completely abandoning the CubeSat form factor, or an adapter must be constructed. With the desire to keep NPS-SCAT within the CubeSat Design Specification, a second structure was developed, designated NPS-SCAT++. This structure has several purposes: to house the NPS-SCAT CubeSat during launch, filling the entire volume of the SSPL-5510; release the NPS-SCAT CubeSat after its own deployment from the Space Shuttle; and act as its own self-contained satellite with the same solar cell array testing components as in the CubeSat, but also incorporating other NPS-designed, SERB-approved experiments such as risk mitigation experiments for TINYSCOPE's attitude and determination control subsystem (ADCS).

The NPS-SCAT++ structure and subsystem arrangement have undergone many iterations, having been developed in parallel with the NPS-SCAT CubeSat [44]. Several parts of the CubeSat had to be modified so that they could be interchangeable with the NPS-SCAT++ configuration, with design changes mostly affecting the solar panels and the placement of external protrusions. The primary consideration in the construction of the NPS-SCAT++ structure was the need to survive the applied loads delivered by the

SSPL-5510 during launch. The SSPL-5510 places a 3,115 N (700 lb) force on the payload internal to the SSPL-5510 structure [45]. NPS-SCAT++ is designed to withstand this force and provide a safe environment for the NPS-SCAT CubeSat.

At the time of this writing, the development of the NPS-SCAT++ nanosatellite has been put on hold as the launch opportunity onboard the Space Shuttle appears to be unavailable. However, STP has offered the NPS-SCAT CubeSat another launch opportunity onboard the first launch of the Falcon 1e launch vehicle. The Falcon 1e is a commercially developed launch vehicle designed by SpaceX, offering larger primary payload volume and mass capability and replaces the older Falcon 1 LV [46]. NPS-SCAT has been slated to launch from a P-POD-like deployer developed by NASA Ames Research Center, known as an Ames Dispenser.

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III. SUBSYSTEM REQUIREMENTS, DESIGN, AND DEVELOPMENT

A. COMMAND AND DATA HANDLING SUBSYSTEM

The command and data handling (C&DH) subsystem of a satellite is critical to the success of the mission and must perform several major functions: receive, validate, decode, and distribute commands to other spacecraft systems and gather, process, and format spacecraft housekeeping and mission data for downlink or for use onboard [47]. Part of the COTS CubeSat Kit (CSK) developed by the United States-based Pumpkin Incorporated, the FM430 Flight Module single-board computer printed circuit board (PCB), seen in Figure 14, will function as the C&DH subsystem onboard NPS-SCAT. The CubeSat Kit was chosen for its self-contained capability and its flight heritage, having been successfully flown in space on the Colombian Libertad-1, Dutch Delfi-C3, Turkish ITUpSAT1, and HawkSat-1 developed by Hawk Institute for Space Sciences [48].

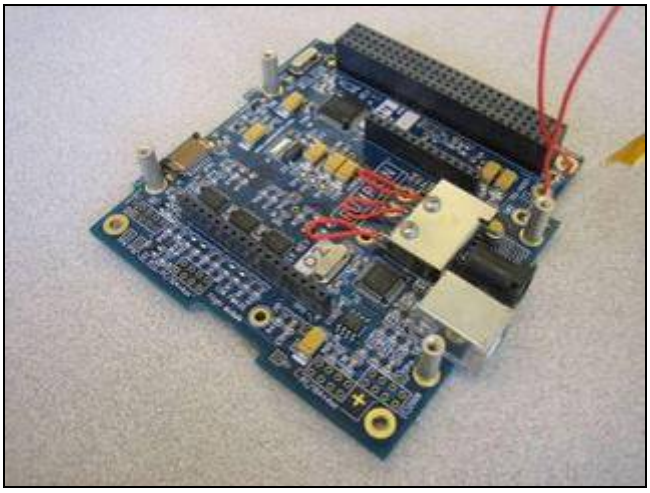

Figure 14 Pumpkin FM430 PCB

A Texas Instruments 16-bit MSP430F1612 is the ultra-low power microcontroller which serves as the “brain” of the satellite. The MSP430 has 55 kilobytes of Flash memory and five kilobytes of RAM. There are 48 general purpose input-output (GPIO) pins which can be allocated to interface with hardware [49]. Using software coded in the

C programming language and through physical hardware connections, the CSK bus, the FM430 communicates to all subsystems. The flight software utilizes the Salvo Real-Time Operating System (RTOS), which provides a versatile software architecture.

The CubeSat Kit uses a stackable 104-pin CubeSat Kit Bus Connector allowing for a wire-free connection between stacked boards inside NPS-SCAT. Two separate 52-pin connectors make up the CSK Bus Connector. When viewing the connectors from above, as shown on a CSK-form factor PCB in Figure 15, the left-most connector is labeled H1 and the right-most connector is labeled H2. The left-hand side of each connector has odd-numbered pins; the right-hand side has even-numbered pins. The top, left corner of the each connector is pin one. Individual pins are referred to first by the connector type, either H1 or H2, and then by their location within the connector; for example: H1.20 refers to pin 20 on the H1 connector.

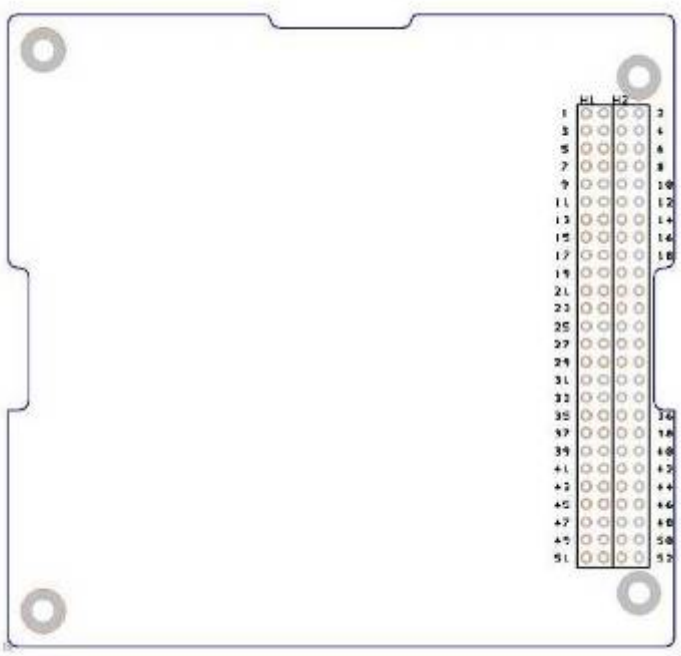

Figure 15 CSK PCB with Labeled Connectors

The FM430 also has a PC/104 footprint that utilizes established circuit board standards permitting already developed circuits to be incorporated into the CubeSat form factor. The 104-pin CSK Bus Connector not only includes all 48 MSP430 GPIO lines

but also incorporates space for user-defined, input-output signal lines and interfaces to other subsystems, including the communications and electrical power subsystems. A Secure Digital (SD) card socket is attached to the bottom of the FM430, enabling onboard storage of up to two gigabytes of data. There is a USB 2.0 connector installed on the FM430 that provides the ability to charge the battery, part of the electrical power subsystem, and interface with the MSP430 microcontroller during development and checkout prior to flight. Other important pieces of hardware located on the FM430 are the Remove-Before-Flight (RBF) switch, or Pull-Pin, and the Launch, or Separation, switch, which are used for connecting and isolating the battery from the charging circuitry and voltage regulators within the EPS.

B. COMMUNICATIONS SUBSYSTEM

The primary purpose of the communications subsystem employed in NPS-SCAT is to provide an "interface between the spacecraft and ground systems" [50]. NPS-SCAT will have two separate entities that comprise the communications subsystem: a primary radio transceiver and a secondary beacon. With two different systems, the satellite will have some redundancy in this important subsystem, which significantly increases the chance of a successful mission.

1. MHX-2400

Complementary to the CubeSat Kit, the MHX-2400 transceiver developed by Microhard, Inc was chosen to be the primary communications radio for NPS-SCAT after first ruling out the newer MHX-2420, as discussed by Schroer in [40]. Operating in the S-band at 2.44 GHz, the MHX-2400 will allow the satellite to establish a wireless connection with the ground station located on the NPS campus in Monterey, California to downlink the primary telemetry. The MHX-2400 is a frequency-hopping, spread-spectrum (FHSS) module that has a maximum output power of one watt, originally intended for terrestrial wireless communication [51]. It was chosen because of its interoperability with the CubeSat Kit as well as its flight heritage, "having been successfully used with GeneSat1 from NASA and MAST from Tethers Unlimited Inc" [41, 43]. A complete link budget was calculated for the primary radio, and despite the

fact it was for the newer MHX-2420, it is still valid due to the use of the same one watt transmit power [40]. As shown in Figure 16, the physical component comprising the MHX-2400 radio is fitted onto the FM430 in specially constructed connectors designed explicitly for this purpose. With this hardware interface, the software controls the data flow to and from the radio.

Figure 16 MHX-2400 (separate and installed in FM430)

The signals transmitted from the radio are sent through a coaxial cable to a Spectrum Controls PA28-2450-120SA patch antenna, which "is essentially a metal conducting plate suspended over a ground plane by a substrate" [40]. The patch antenna produces a right-handed circularly polarized signal with sufficient gain in all directions to close the link between NPS-SCAT and the ground station [40]. A prototype panel showing the desired mounting of the patch antenna with a copper ground plane is shown in Figure 17.

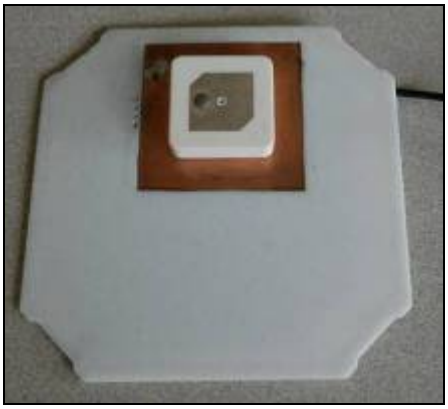

Figure 17 Patch Antenna Mount (From [40])

2. Beacon

The secondary communications system operates within the amateur band, 430-438 MHz, and is being developed as a joint venture between NPS and Cal Poly. This system will function primarily as a beacon, transmitting secondary telemetry consisting of system health parameters and a packet of payload data; it will also receive command uplinks from NPS for satellite housekeeping. Although the beacon has flight heritage, having been flown on the CP-series of satellites developed by Cal Poly, it is being reformatted to work with the CSK bus. The Cal Poly-designed beacon circuit board is being built to be within the PC/104 form factor, allowing it to take a slot within the NPS-SCAT structure and fit onto the CSK Bus Connectors. It will interface with the FM430 using a dedicated inter-integrated circuit (I^2C) bus. Located on this PCB is the circuitry needed to transmit on the amateur band and packetize the data with an AX.25 data link layer protocol. Attached to one of the sides of NPS-SCAT is a half-wave dipole antenna that is used by the beacon to transmit and receive signals with two quarter-wavelength radiating elements. Prior to launch, the beacon antenna will be stowed in a Delrin structure designed to allow the satellite to meet the CDS [1]. Software will command circuitry to deploy the antenna after a preset time when the satellite has exited the launch vehicle. Figure 18 shows the satellite's beacon antenna structure with a deployed antenna.

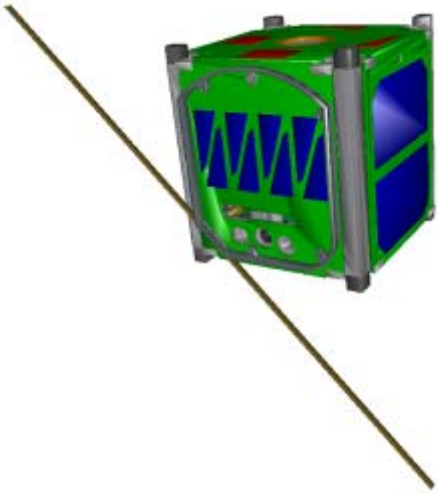

Figure 18 NPS-SCAT with Beacon Antenna Structure and Deployed Antenna

C. ELECTRICAL POWER SUBSYSTEM

The electrical power subsystem (EPS) of the NPS-SCAT satellite is used to provide, store, distribute, and control the spacecraft electrical power [52]. The electrical power subsystem suite onboard NPS-SCAT is composed of six solar panels that feed power to a Clyde Space 1U EPS, which holds a 1U battery daughter board consisting of two lithium polymer cells.

1. Clyde Space 1U EPS1

At the beginning of the NPS-SCAT program, there were a limited number of manufacturers producing CubeSat-sized power systems. The EPS developed by Clyde Space, a company based out of Glasgow, Scotland, was chosen for use on the satellite. During the development cycle of NPS-SCAT, more and more CubeSat developers have chosen the Clyde Space EPS. The power system technology developed at Clyde Space has previously been flown on larger satellites including the Surrey Satellite Technology Limited (SSTL) nanosatellite SNAP-1 (Surrey Nanosatellite Applications Platform), the Turkish RASAT (a Turkish word meaning "observation"), and the United States Air Force Academy's FalconSAT-2. The University of Texas used the Clyde Space 1U EPS on their BEVO1 satellite, also known as PARADIGM (Platform for Autonomous Rendezvous And Docking with Innovative GN&C Methods), which launched along with its sister satellite developed by Texas A&M University, AggieSat2, on 30 July 2009 during the STS-127 mission, giving the Clyde Space 1U EPS flight heritage [53].

The battery daughter board holding two lithium polymer cells is stacked directly on top of the EPS and is secured with four bolts, three of which are electrically ground and the fourth is the full battery voltage (VBAT). The EPS is designed to be compatible with the Pumpkin CubeSat Kit and is in the same PC/104 PCB form factor with the complete 104-pin CubeSat Kit Bus Connector, allowing for a simple stackable integration. A picture of the 1U EPS with the battery daughter board is shown in Figure 19.

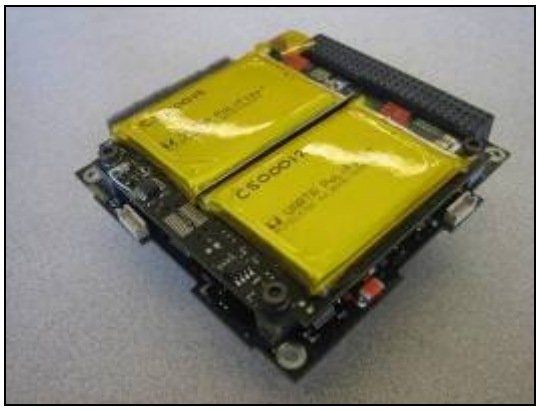

Figure 19 Clyde Space 1U EPS1 with Battery Daughter Board

At the heart of the circuitry is the Battery Charge Regulator (BCR), which takes as an input the power generated by the solar panels and outputs the voltage and current required to charge the battery. There are a total of three BCRs on the EPS, one for each axis of solar arrays (±x, ±y, and ±z). The voltage provided to the BCRs must be between 3.5 V-10 V at current not to exceed 0.5 A; the solar panels must be designed to meet this specification. The BCRs use a maximum power point tracker (MPPT) to actively monitor "the characteristics of the solar array and set the BCR input voltage to the maximum power point of the array" [54]. To produce enough power to charge the battery, the voltage is stepped to the proper level using a single ended primary inductor converter (SEPIC), resulting in a 90% efficient charge operation when the BCRs are operating with a full load. This charge efficiency was empirically determined by Dorn in [42]. The EPS provides a 5 V and a 3.3 V regulated bus, both of which use a simple buck converter to step down the battery voltage. The operational battery voltage varies from 6.4 V to a maximum of 8.2 V. There is also an onboard processor that sends telemetry to the FM430 via a dedicated I^2C bus and provides information such as battery voltage and current, battery temperature, solar panel voltage and current, and power usage data. The USB input on the FM430 provides a +5 V power source that feeds into BCR1, allowing the USB interface to charge the battery, shown in Figure 20. The battery is isolated from the BCR and voltage regulator buses via the Pull-Pin and Separation Switch, respectively. When the Pull-Pin (RBF pin) is installed, the Pull-Pin switch is open; this prevents the BCRs from draining the battery with its small constant parasitic current of approximately

1.21 mA, determined by Justin Jordan in [55]. When the Separation Switch is closed (and the Pull-Pin is pulled out, closing the switch), the EPS has an additional 49.4 mA parasitic load due to the voltage regulators [55]. This data was used to calculate the power budget for the satellite and the power needed to be produced by the solar panels [42].

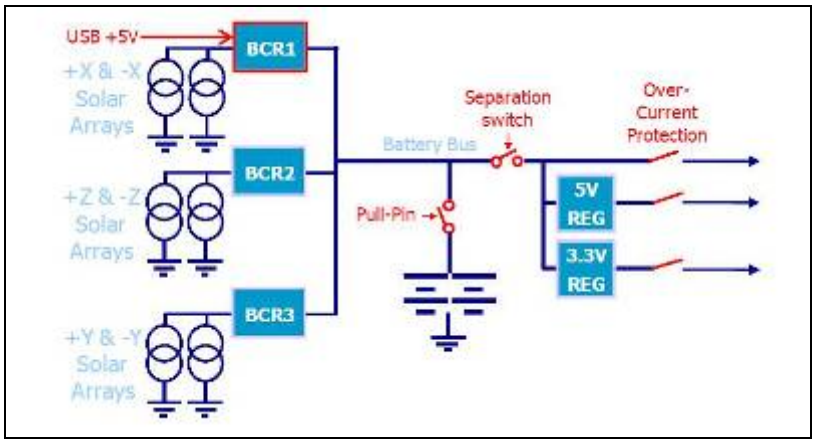

Figure 20 Clyde Space 1U EPS1 Schematic (From [54])

The problems with Clyde Space's first version of the 1U CubeSat electrical power subsystem, designated as EPS1, include the inability to power the MHX-2420 transceiver, lack of proper documentation from the manufacturer, and the parasitic load experienced when the Pull-Pin is removed. Other issues with this revision, as identified by other Clyde Space customers, include poor quality build and conformal coating, launch switch configuration difficulties, over-discharge of battery, incompatible or inoperable battery protection circuitry, and accidental short-circuit of battery due to improper safety precautions [56]. Clyde Space has responded with a newer revision, the EPS2, which has hopefully corrected these issues. The remainder of the document refers to the first version, the Clyde Space 1U EPS1.

2. Solar Panels

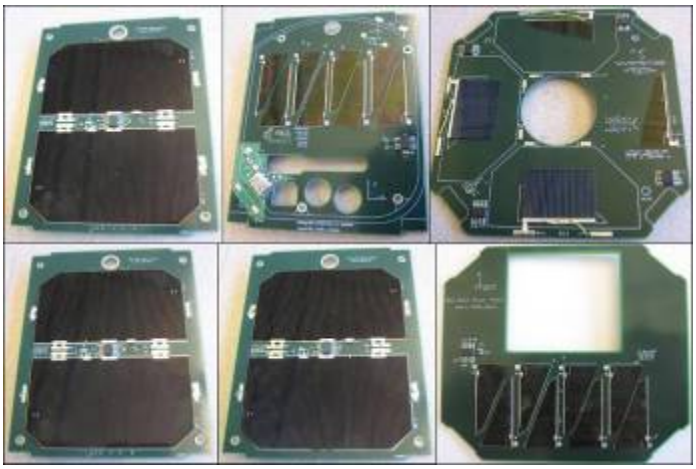

Figure 21 NPS-SCAT Solar Panels (l to r: top row: +x, +y, +z; bottom row: -x, -y, -z)

The six solar panels make up the sides of the satellite, were developed together by Dorn, Jordan, and the author, and are shown in Figure 21. The primary solar cells used to produce power are Spectrolab Improved Triple Junction (ITJ) Cell-Interconnect-Coverglass (CIC). Each of the ITJ CIC solar cells is 26.8% efficient and produces approximately 2.3 V at 0.5 A in an air mass zero (AM0) environment [32]. The coverglass on these cells protects them from the harsh space environment including cosmic radiation and other atomic particles. The +x-, –x-, and –y-axis solar panels each have two of the ITJ CIC solar cells in series to produce around 5 V at 0.5 A, about 2.5 W per panel. The +y- and –z-axis solar panels have reduced area due to other components (the +y-axis panel has the beacon antenna structure, matching circuitry, and FM430 access ports; the –z-axis panel has the MHX-2400 patch antenna) which necessitate a different sized solar cell to maximize power collection. These cells are the Triangular Advanced Solar Cells (TASC), have a smaller more unique triangular shape, and are also manufactured by Spectrolab. The TASC are Ultra Triple Junction (UTJ), have an efficiency of 28.3% but do not have any coverglass [57]. They produce about 2.5 V but, due to their reduced area, produce a smaller amount of current, around 35 mA in an AM0 environment. A total of eight TASC are used on each of the +y- and –z-axis solar panels; two sets of four cells are placed in parallel, with the four cells in each set placed in series. A circuit schematic of this configuration is seen in Figure 22. The experimental solar

panel (ESP) is located on the +z-axis face and contains the four experimental solar cells. When they are not being tested by the solar cell measurement system (SMS), the power produced by the experimental solar cells is being fed to the EPS like the rest of the solar panels. However, with the present design of the experimental solar panel, the voltage level produced by the experimental solar cells is too low to power the BCRs on the EPS, and thus cannot be used for satellite power production. A future revision of the ESP could be constructed to provide the full functionality built into the design and deliver power to the EPS.

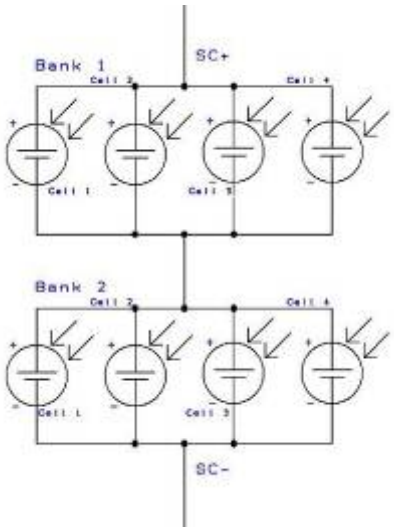

Figure 22 TASC Configuration Circuit Schematic

The power solar panels also contain digital temperature sensors to monitor the satellite's temperature on all faces. Each panel, with the exception of the ESP, has two temperature sensors: one on the outer side, one on the inner side. The experimental solar panel has a total of four temperature sensors corresponding to each experimental solar cell.

D. THERMAL CONTROL SUBSYSTEM

The purpose of the thermal control subsystem is to "maintain all spacecraft and payload components and subsystems within their required temperature limits" [34]. The importance of this subsystem is noted when one realizes the environment in which the satellite must survive varies significantly between the two hot and cold extremes. NPS-

SCAT has a passive thermal control subsystem (TCS), using the built-in coatings of the external materials and components. An analysis to model the thermal environment experienced by the satellite was conducted to validate the use of a passive TCS for NPS-SCAT and is documented below.

A simplified model of the NPS-SCAT satellite was developed assuming the entire satellite was one thermal node. Using the overall surface area of the satellite, an equivalent sphere was calculated to form the single node. The power usage of each subsystem was taken from the power budget and used for the total equipment power dissipation value. The actual emissivities, absorptivities, and heat capacities for each of the three primary materials comprising the satellite (aluminum, solar cells, and FR-4) were combined based upon mass distribution to find a single node value for each characteristic. The basic fourth-order temperature equation was simplified down to a linear relationship, producing an upper and lower temperature that is experienced by the satellite throughout a given orbit [58].

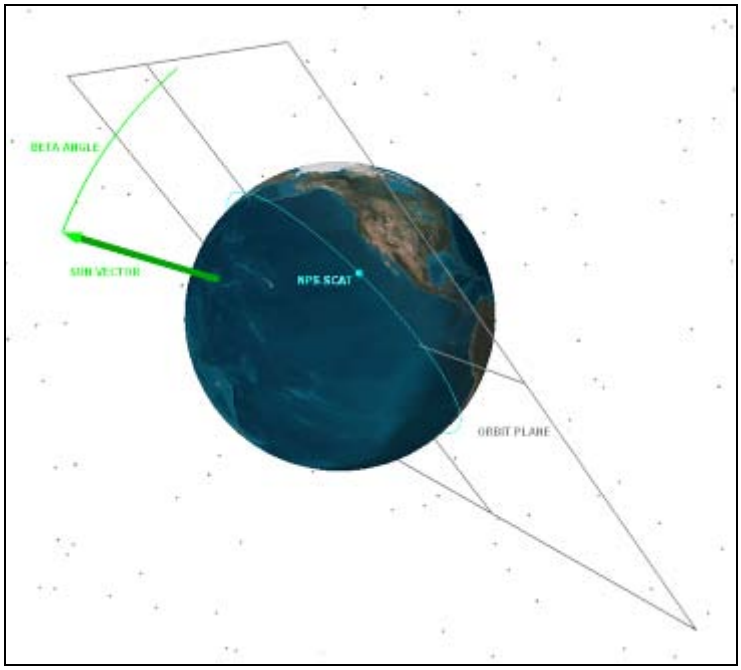

Figure 23 Sun-orbit, β, Angle Definition

The sun-orbit angle, or β angle, is defined as the angle between the sun vector and the orbit plane, as seen in Figure 23. For a given orbit, the β angle varies throughout the year. The relationship between the β angle and time is generally sinusoidal and is orbit specific, varying between the values of the orbit inclination ± 23.4° [59]. "As viewed from the sun, an orbit with β equal to 0 deg appears edgewise… [w]ith β equal to 90 deg, a circular orbit appears as a circle as seen from the sun; no eclipses exist" [59].

Two orbits were considered for the TCS single node analysis. The first assumed orbit was circular with an altitude of 336 km, 10 km below the International Space Station (ISS) altitude, and with an inclination of 51.6°. This orbit was chosen based upon the possible flight opportunity onboard the Space Shuttle. Figure 24 depicts the change in the β angle for NPS-SCAT while in this orbit over the course of a year, which varies between approximately ±75°.

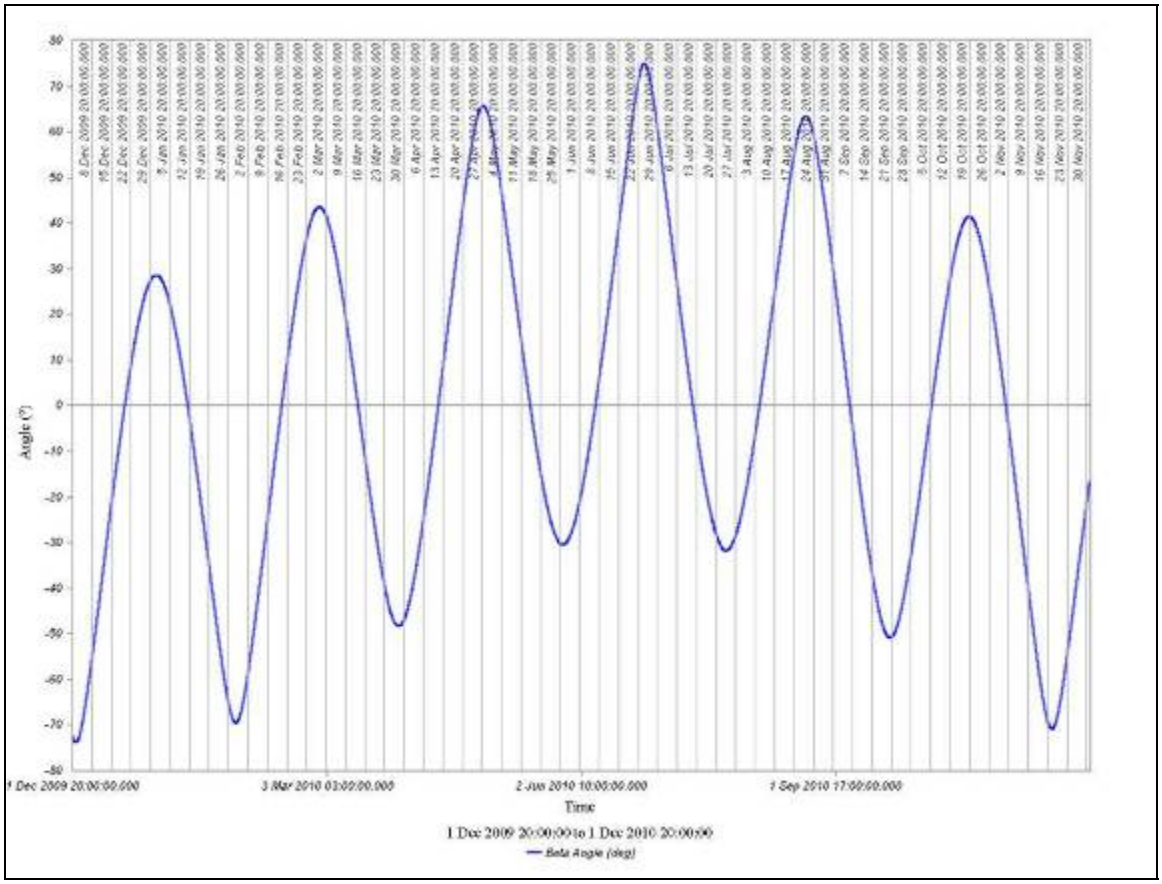

Figure 24 NPS-SCAT β Angle Year-Long Variation, Space Shuttle Orbit

With a β angle of zero degrees, indicating a maximum eclipse time, the satellite will experience the largest temperature swing. For a single node model representing NPS-SCAT with a β angle of zero degrees, the calculated extreme temperature values were 46°C and –16°C. When the β angle was increased, these two values began to equalize and eventually reach equilibrium at the point where the satellite no longer experiences an eclipse. This event occurred when the β angle was greater than 72° and NPS-SCAT received continuous sunlight. A thermal steady-state was achieved with an overall satellite temperature of about 58°C. As β approached 90°, the overall spacecraft temperature dropped; this was due to cosine relationship between β and the earth's albedo and was one of the assumptions made within the single node model. However, due to the limitations of β for this orbit, the change in satellite temperature was very small upon entering full sunlight. A plot of the temperature versus β angle, displaying the upper and lower temperature limits for the single node thermal model, is shown in Figure 25.

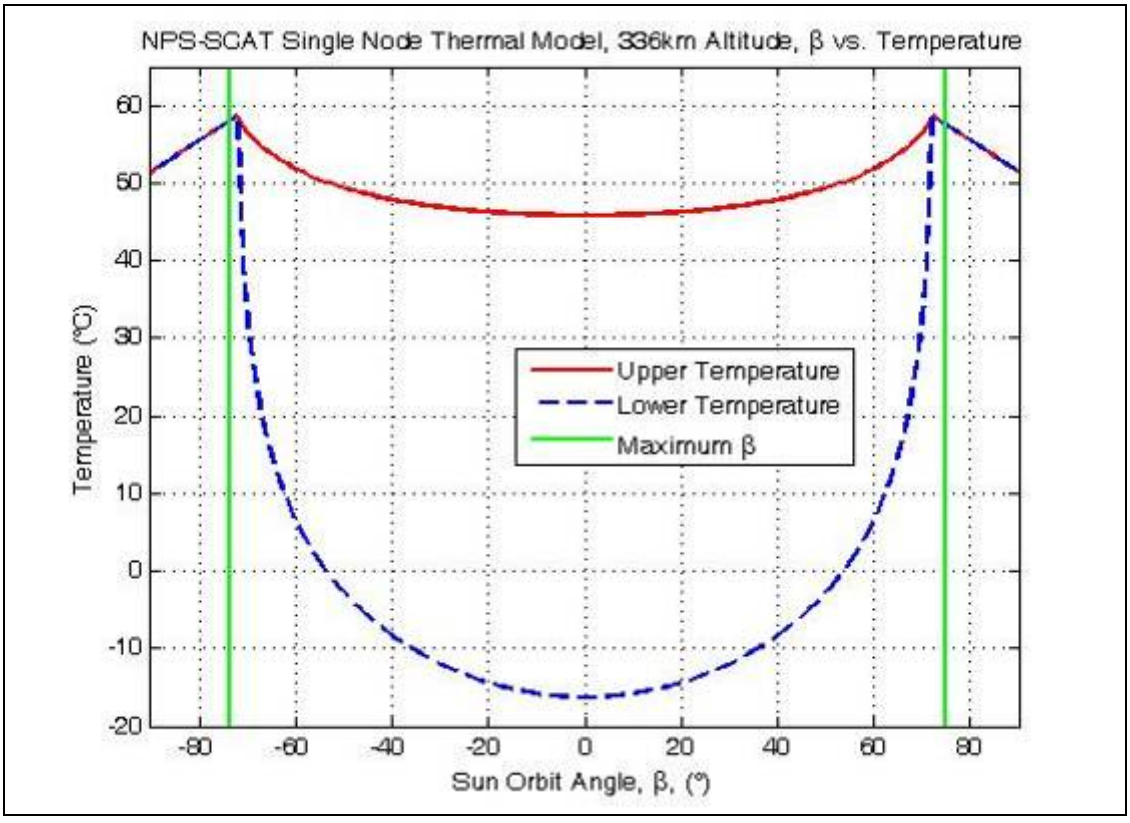

Figure 25 Single Node Thermal Model β Angle vs. Temperature, Space Shuttle Orbit

The same single node model was re-run using data for a second assumed orbit, based on what the first Falcon 1e launch is expected to reach. This orbit is circular with a minimum altitude of 450 km and an inclination of 45°. The updated temperatures resulted in a very slight increase in temperature swing, with extreme temperatures of 47°C and -15°C. A thermal steady-state for NPS-SCAT in this orbit was never achieved due to the fact that the satellite always experiences an eclipse. This can be seen by the green lines marking the maximum β angle experienced for the Falcon 1e orbit in Figure 26 and was also confirmed with an orbit simulation in Satellite Tool Kit (STK). Despite never achieving a thermal steady-state, the maximum temperature the satellite experienced was 56°C. It should be noted that the extreme values of the two different orbits do not differ greatly. The next two figures depict the resulting β angle vs. time and β angle vs. temperature, respectively, for the Falcon 1e orbit.

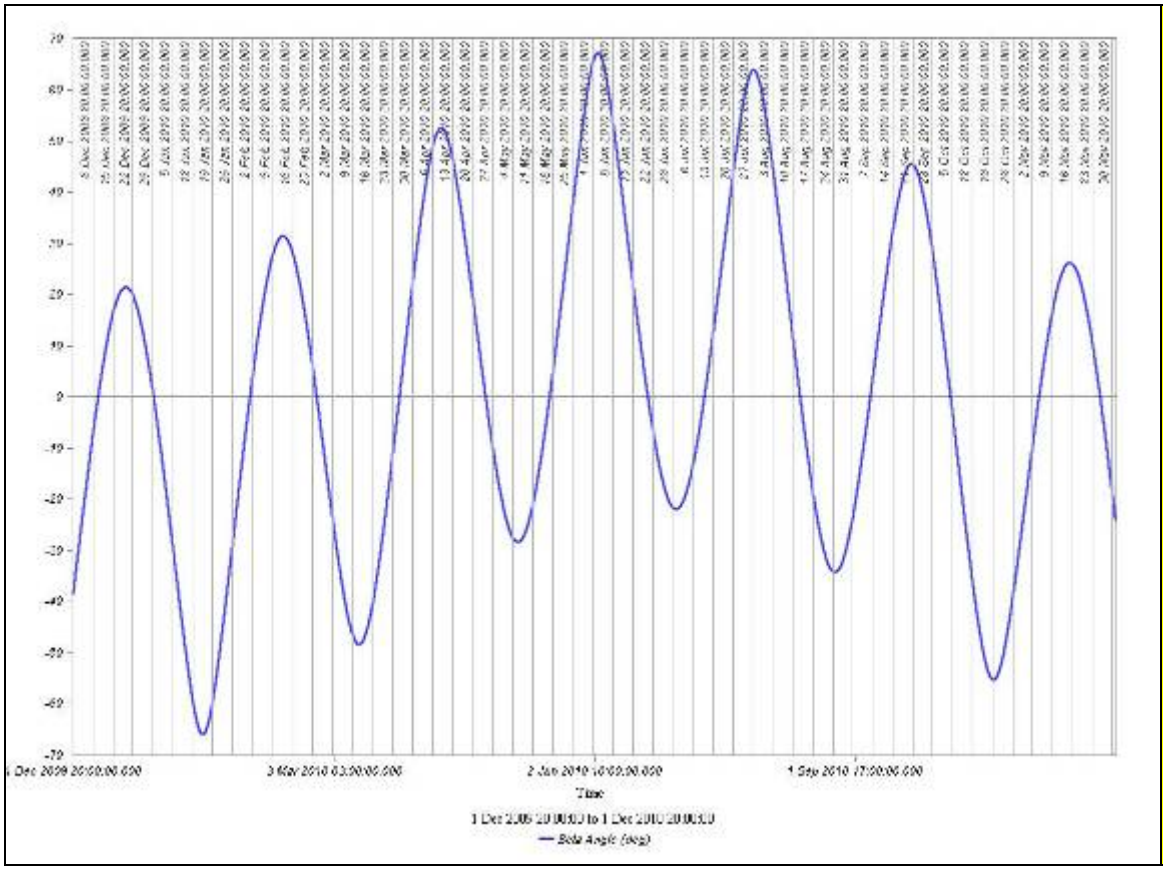

Figure 26 NPS-SCAT β Angle Year-Long Variation, Falcon 1e Orbit

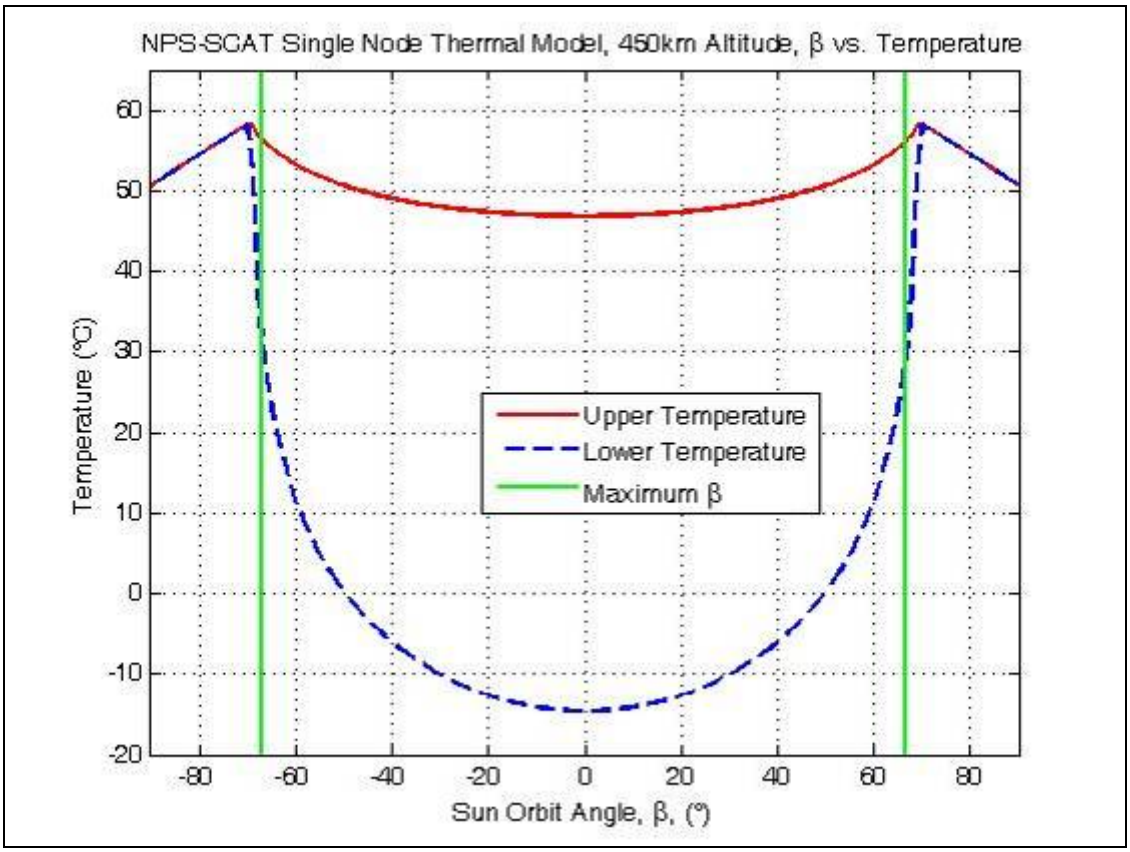

Figure 27 Single Node Thermal Model β Angle vs. Temperature, Falcon 1e Orbit

The single node model is not the most accurate model for thermal analysis but is useful in developing an idea of the type of thermal environment in which the satellite must survive. It also is a stepping-stone on which to construct a more comprehensive thermal model of the spacecraft. Due to the simplistic nature of this model, several assumptions were made, including aggregating the CubeSat shape into a sphere with equivalent surface area and mass and keeping certain variables constant. However, the assumption that had one of the biggest effects on the end result, the upper and lower temperature limits, was the calculation of the absorptivities and emissivities. Based upon the results of the single node analysis, the satellite will not experience any temperatures that are greater than the maximum operating temperature of any component, including the EPS battery. Using only this model, the satellite would not require any extra elements added to maintain a satisfactory internal temperature. A more comprehensive model using more than one node would take into account the actual satellite shape,

internal configuration, extensive orbit modeling, and would no doubt provide a more realistic range of temperatures, but is beyond the scope of this thesis.

E. PAYLOAD

The payload of NPS-SCAT is a solar cell measurement system (SMS), which consists of circuitry used to measure experimental solar cell current, voltage, temperature, and the sun angle that the solar cells experience. The SMS circuitry uses input commands sent in the form of voltage signals from the onboard microcontroller through a digital-to-analog converter (DAC) to control the solar cell current. The solar cell current is related to the load current density, J_L, in the solar cell equivalent circuit in Figure 9. The input voltage from the DAC is divided by a resistance value, tailored to the specific experimental solar cell, resulting in the solar cell current. The output of the SMS circuit, solar cell voltage, is read by an analog-to-digital converter (ADC) and stored onboard the satellite for later transmission. The solar cell voltage correlates to the load voltage, V_L, in the solar cell equivalent circuit in Figure 9. When plotted, the points produced by the SMS circuitry form an I-V curve, or solar cell current versus voltage plot. Seen in Figure 28 is an example plot of I-V and power curves with key points labeled that help classify a solar cell's performance: short circuit current, I_{SC}; open circuit voltage, V_{OC}; and maximum power, P_{MAX}.

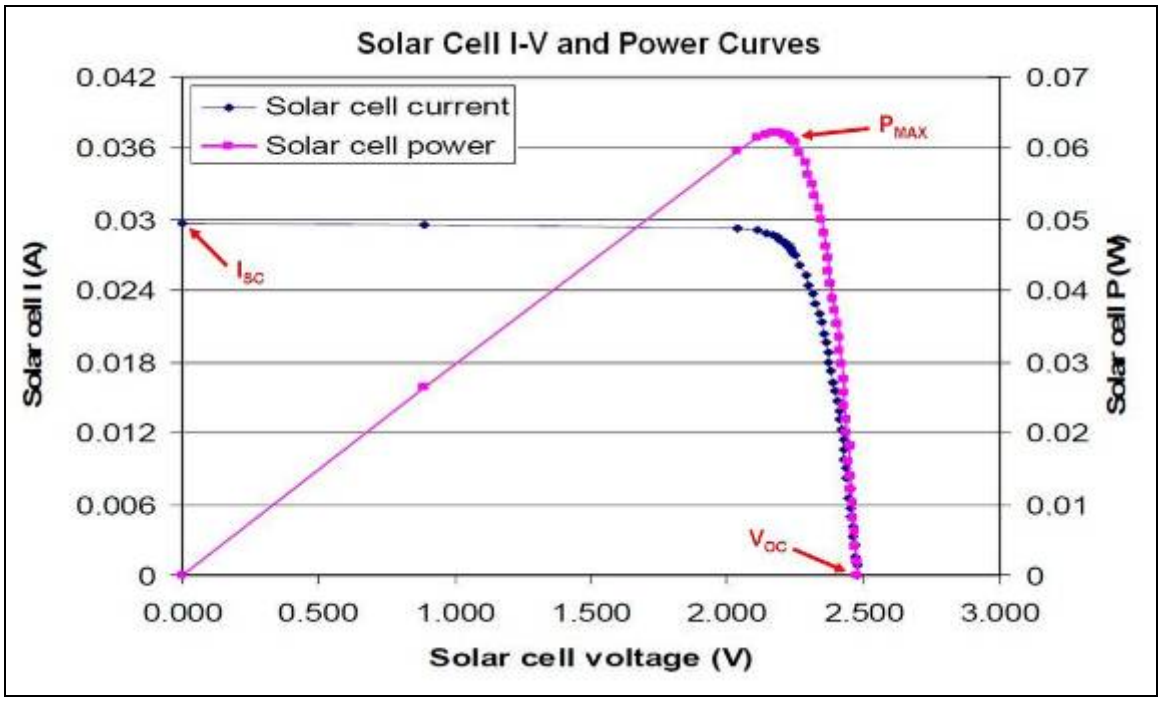

Figure 28 Example I-V Curve (After [39])

In addition to measuring the solar cell current and voltage, information such as sun incidence angle and temperature are also required to complete a full analysis of solar cell performance. Temperature and sun incidence angle are the major environmental factors that will be measured by the NPS-SCAT satellite as they cause the apparent solar cell performance to fluctuate significantly. Radiation and atomic oxygen, as mentioned previously, are sources of solar cell degradation and their effects will be measured indirectly through the experimental solar cell output characteristics.

The geometric shape of NPS-SCAT is a cube with six faces; one of the faces, defined as the positive z-axis, contains the experimental solar panel. On this panel are located the experimental solar cells and corresponding digital temperature sensors; the center of the panel contains an aperture for the sun sensor. Digital temperature sensors are placed on the experimental solar panel to measure each experimental solar cell's temperature. Because the satellite is planned to be in a low earth orbit, causing the thermal environment to vary considerably throughout its orbit, the temperature sensors provide the solar cell temperature and help assess the I-V curve data. As defined

previously in chapter two and shown in Figure 11, the sun angle is measured between the surface normal and the incident light ray and will cause decreased solar cell current output as the angle increases. Using the onboard Sinclair Interplanetary SS-411 digital sun sensor, which has a ±70° field of view and ±0.1° accuracy, this angle can be measured, the effective current calculated, and the temperature data factored into the analysis of the I-V curve data. The I-V curve data points can then be correlated to a database of known current and voltage values at given sun angles and temperatures. Over time, solar cell degradation can be quantitatively determined [43].

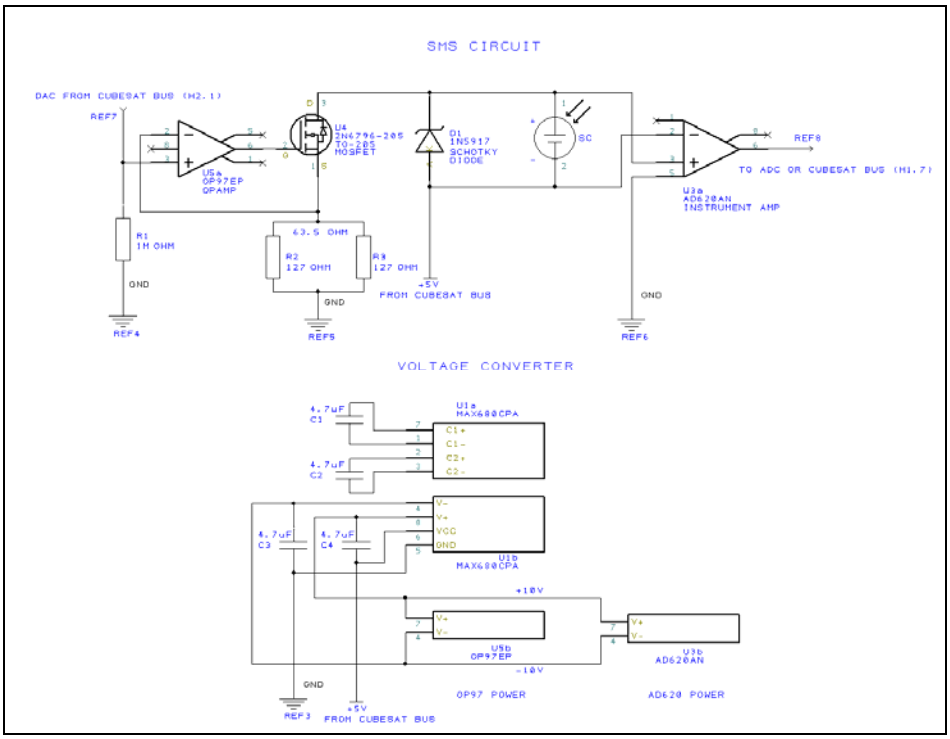

Figure 29 SMS V0 Circuit Schematic

1. SMS Version Zero

The solar cell measurement system developed for NPS-SCAT originated from a similar circuit designed for another NPS spacecraft, NPSAT1. The original circuit was developed as an autonomous circuit to measure characteristics of individual photovoltaic devices in space [31]. This circuit was then modified for use with a microprocessor and a control system to automatically measure the parameters of several solar cells [60]. The microprocessor-based control system was implemented for use onboard NPSAT1 as one

of the experiments [61, 62]. The NPS-SCAT prototype SMS circuit, shown in Figure 29, was modeled off of the NPSAT1 design, miniaturized, and placed onto a Pumpkin CubeSat Kit prototyping circuit board by Bein to fit within the CubeSat form factor using discrete components and point-to-point wiring as shown in Figure 30. The resulting system has been designated SMS Version Zero (V0) as part of the naming convention for the various versions of SMS circuit boards developed for NPS-SCAT.

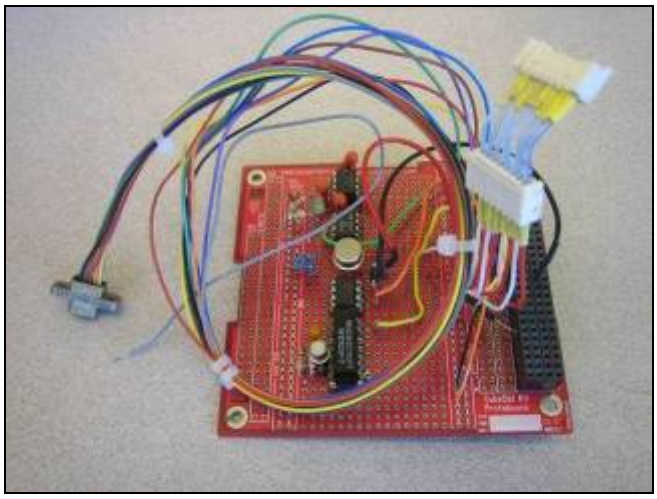

Figure 30 SMS V0 Prototype Circuit Board (After [39])

The SMS V0 circuit consists of several discrete components that enable the circuit to function. An OP97 operational amplifier accepts the DAC voltage input at its positive terminal, with the negative terminal providing feedback from the source of the 2N6796 MOSFET. The MOSFET source is connected to a resistance of 63.5 Ω for testing TASC, determined using the maximum expected output current of the solar cell. The OP97 op-amp output is connected to the gate of the MOSFET. The drain of the MOSFET is connected to the solar cell to be tested as well as a Schottky rectifier, which prevents the solar cell from being reversed-biased. The OP97 acts as the switch controller, opening the MOSFET to allow the requisite amount of current to flow based upon the DAC input voltage and resistance values. The +5 V pedestal bias voltage ensures enough voltage across the MOSFET for proper operation; this bias could be as low as 1 V but further testing would be required before making any changes to the design. The current value, which is the solar cell current, is determined by Ohm's Law using the DAC voltage and

resistance value. The solar cell voltage required to produce this current is measured by the AD620 instrumentation amplifier, which outputs the voltage difference between its two input pins. Both amplifiers, the OP97 and AD620, require a ±10 V power supply in order to operate properly. The CubeSat Kit and Clyde Space EPS were designed to produce only a maximum voltage of +5 V, thus creating the requirement for a voltage converter. A MAX680 voltage converter was used to provide the necessary ±10 V. Due to the power limitations of a 1U CubeSat, most components were chosen based upon their low power consumption.

The signal that controls the output of the SMS circuit is sent from the DAC on the FM430. The DAC has been configured in the software to cycle through voltage levels from zero to 2.5 V, with the load resistance setting the current. For data analysis, the DAC value, a voltage, is divided by the resistance value of the resistor fitted in the SMS circuit. The resistance value sets the amount of solar cell current. For the prototype, which used UTJ TASC, the maximum expected current was 35 mA. The resistance value was originally set to 63.5 Ω, which sets the maximum current to 39 mA, giving a slight margin for terrestrial use but not enough for when the satellite is in an AM0 environment. The output of the SMS circuit, the solar cell voltage, is then sent to ADC1. The pertinent pins used by SMS V0 on the CubeSat Kit Bus Connector are shown in Table 4

Table 4 SMS V0 Pin Allocation

Net	Use
H2.1	DAC
H2.7	ADC1
H2.25	+5 V
H2.29	GND

2. ESP Version One

The solar cell measurement system is not complete without an experimental solar cell. To have the capability to test more than one solar cell, an entire panel was created. Paired to the SMS V0 prototype circuit board is the Experimental Solar Panel Version

One (ESP V1), was created by Bein and is shown in Figure 31. Because this component was the building block for future design iterations, the following is a brief description to provide the necessary background.

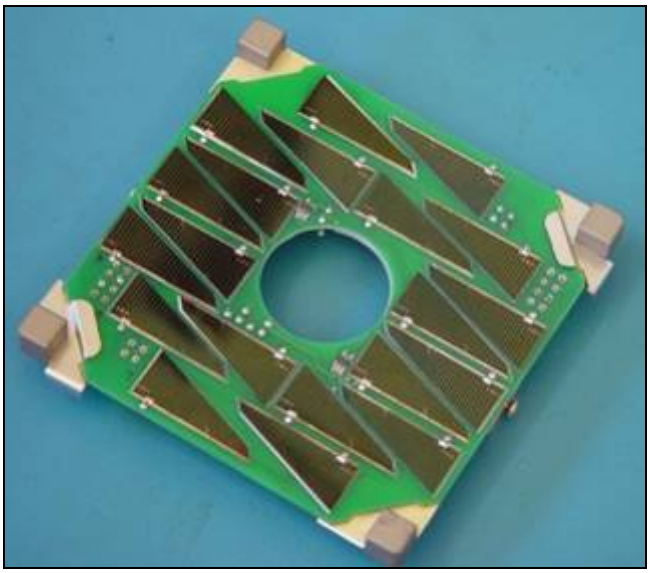

Figure 31 ESP V1 (From [39])

In addition to measuring a solar cell's current and voltage, the SMS V0 prototype circuit board also takes temperature data from sensors located on ESP V1. These components, MAX6630 digital temperature sensors, are connected to the satellite via the serial peripheral interface (SPI) protocol. There are a total of four temperature sensors on the ESP V1. Each temperature sensor requires a separate active low slave select (/SS) control line. The common pins shared between the sensors are master input, slave output (MISO), or just slave output (SO); Serial Clock (SCK); +5 V power source, and ground (GND). A Molex eight-pin connector is used to connect the SMS Version Zero prototype circuit board to the ESP V1. Pin one is indicated by a 'V' notch on the male connector. The listing of CSK Bus Connector pins used by ESP V1 is shown in Table 5.

Table 5 ESP V1 Temperature Sensor Connector Pin Allocation

Pin	Net	Use
1	H2.25	+5 V
2	H2.29	GND
3	H2.24	SCK
4	H2.18	SO
5	H2.23	/SS1
6	H2.22	/SS2
7	H2.21	/SS3
8	H2.20	/SS4

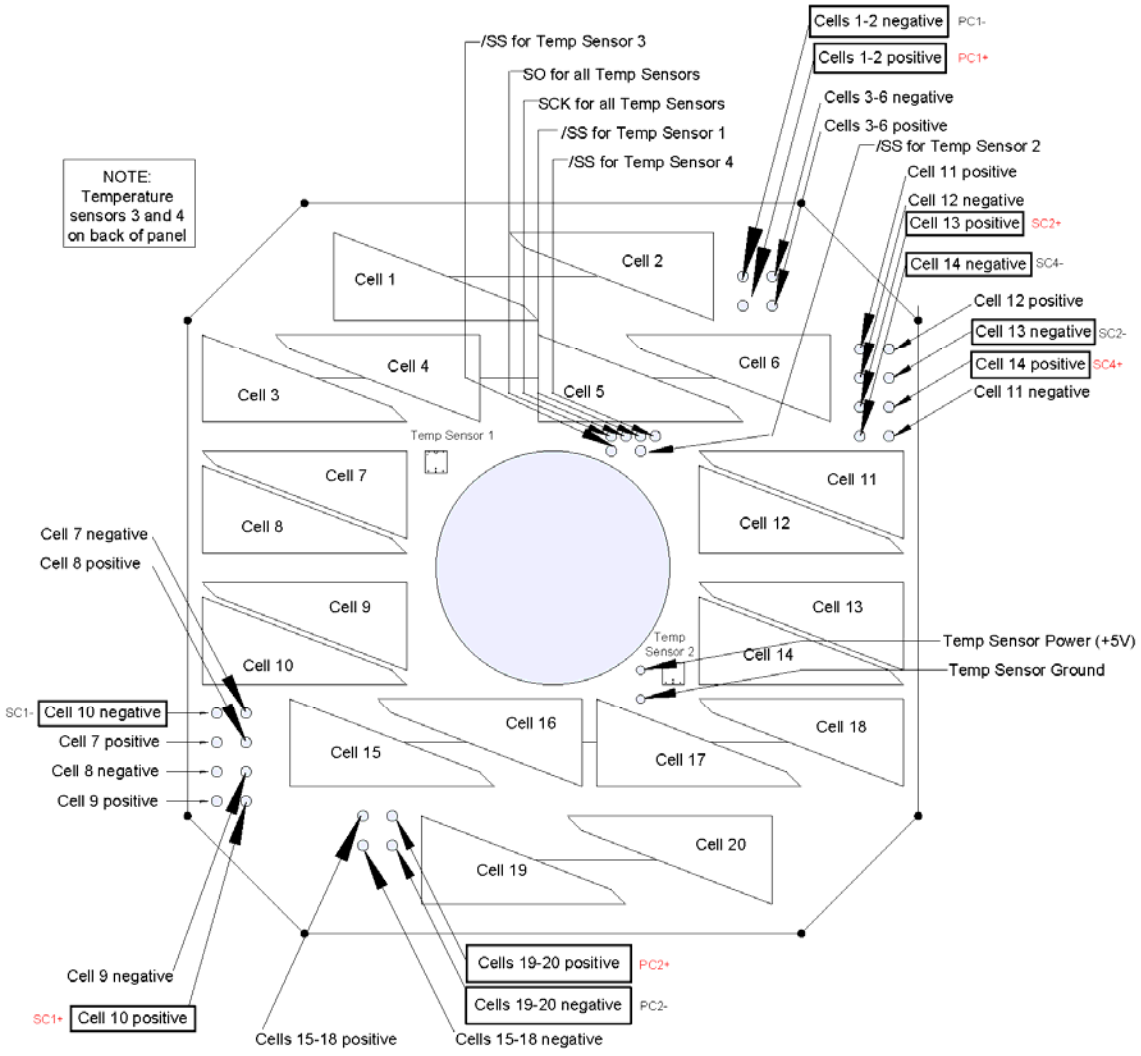

Figure 32 ESP V1 Schematic (After [39])

There are 20 TASC solar cells populating the top layer of the ESP V1. As shown in Figure 32 (edited for minor typographical errors from [39]), cells one and two are connected in series, cells three through six are in series, cells 15 through 18 are in series, and cells 19 and 20 are connected together in series. The remaining cells are left to be accessed individually. Future versions of the SMS PCB have been designed to be compatible with ESP V1 using these cells and will be discussed in further detail for each version of the SMS PCB.

3. Sinclair Interplanetary SS-411 Digital Sun Sensor

A prominent feature of the payload is the digital sun sensor, used for determining the sun angle experienced by the experimental solar cells. It is produced by the Canadian company Sinclair Interplanetary and provides a host of functions including an output of a vector to the sun. The sensor is highly complex and is the most expensive piece of equipment on the satellite at $9,000 for the flight unit. It has a front surface made of sapphire that is mirrored with several slits cut in the reflective material to allow sunlight to pass through an optical filter to an array of photosensors. A microcontroller internal to the sensor controls when the photosensors take readings and computes the sun vector after the photosensor array has conducted its exposure. The sun sensor requires a +5 V input from the satellite for power [63].

The sun sensor is interfaced with the FM430 via the same SPI protocol used by the MAX6630 temperature sensors on the ESP V1. There is an extra control line that is part of the SPI bus and only required by the sun sensor: master output, slave input (MOSI). The remaining lines are the same as described for the temperature sensors. A micro-D connector is mounted directly to the gold-plated aluminum sun sensor body and is connected to the respective control lines on the SMS circuit board with an eight-pin Molex connector. The pins are labeled when looking at the micro-D connector adapter on the sun sensor shown in the configuration below in Figure 33 and are allocated as stated in Table 6. The pin-out is the same for the Molex connector with pin nine being omitted and not used.

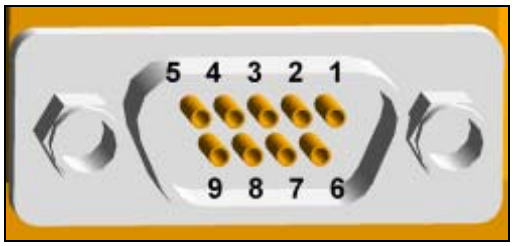

Figure 33 Sun Sensor Connector Pin Numbering

Table 6 Sun Sensor Connector Pin Allocation

Pin	Wire Color	Net	Use
1	Black	H2.29	GND
2	Brown	H2.19	/SS
3	Red	H2.18	MISO
4	Orange	H2.29	GND
5	Yellow	-	NC
6	Green	H2.25	+5 V
7	Blue	H2.17	MOSI
8	Purple	H2.24	SCK
9	Gray	-	NC

The reference frame of the sun sensor is explicitly defined by the manufacturer to avoid confusion when gathering the sun angle and is shown in Figure 34. It

> has a right-hand orthogonal x-y-z Cartesian frame that is developed as follows: the z-axis is normal to the mounting plane, pointing from the spacecraft to the sensor; the y-axis is parallel to the vector running from the center of one alignment pin to the other; the x-axis is perpendicular to the y- and z-axes, pointed generally from the center of the unit towards the electrical connector. [63]

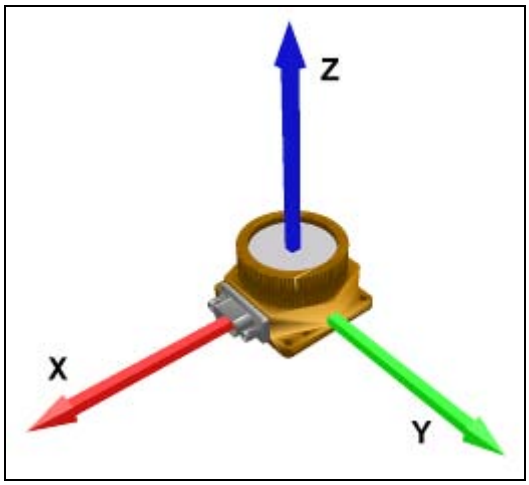

Figure 34 SS-411 Sun Sensor Coordinate System Definition

4. Development of the Circuit Board Configuration

Before moving to a newer version of the SMS, a study of the structural layout of the circuit board was necessary. SMS V0 did not incorporate the sun sensor within its physical layout but instead used a separate board to hold the sun sensor in addition to the SMS V0 circuit board. This configuration did not optimize the limited volume of a 1U CubeSat. It was determined that the sun sensor should be housed either directly on the SMS circuit board or very close by to minimize the volume taken by the payload. Several options were created, first in the CAD (Computer Aided Design) program I-DEAS (Integrated Design and Engineering Analysis Software) and then physically manufactured with ABS plastic using a Stratasys FDM400mc 3D printer.

a. Option One

The first design option for the SMS PCB integrated with the sun sensor was one that put the sun sensor simply mounted on top of the circuit board, shown in Figure 35.

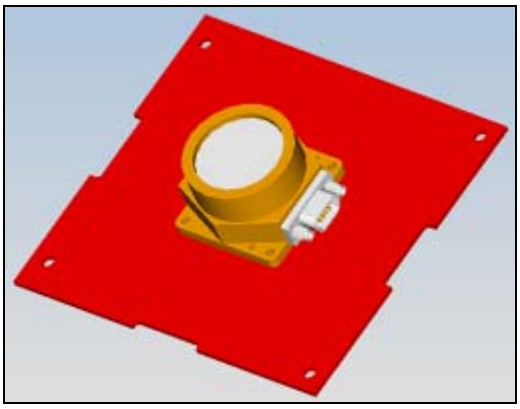

Figure 35 SMS PCB Option One

With this design, the sun sensor is mounted to the circuit board using four #2-56 screws with corresponding washers and nuts. The sensor is placed in the center of the board so as to fit into the hole cut in the +z-axis solar panel. This design somewhat reduces the usable area of the board for circuitry within the sun sensor's footprint. Also, large components cannot be placed near the micro-D connector as they might interfere with the mating interface.

b. Option Two

The second design option for the SMS PCB places the circuit board over the sun sensor so as to reduce the vertical distance between the SMS and the +z-axis solar panel. There is a cut-out in the board for the hexagonal structure of the sun sensor and the micro-D connector as seen in Figure 36.

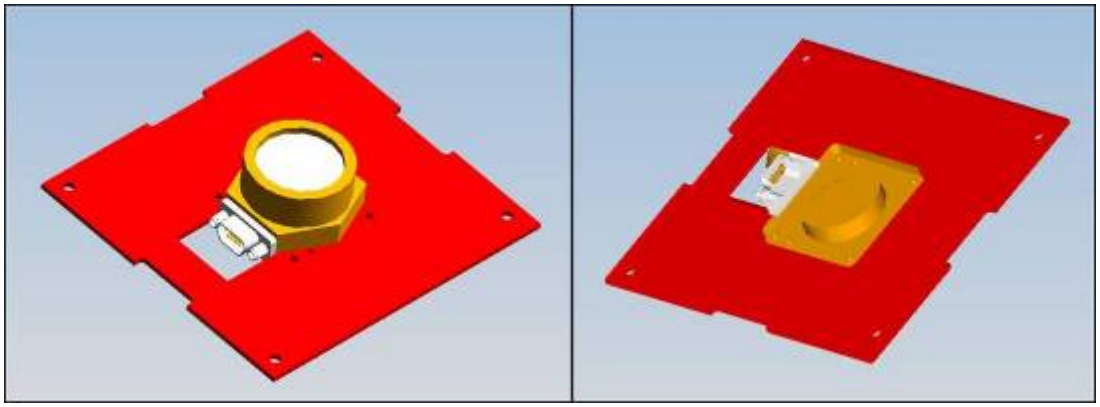

Figure 36 SMS PCB Option Two

The sun sensor is still mounted to the circuit board with #2-56 screws through the drill holes. This design adds a small amount of area to be used for circuitry on the top layer of the circuit board but takes away from the bottom and inner layers due to the cut-out. Also, the notch cut for the micro-D connector reduces the circuit board's overall structural strength.

c. Option Three

The final design option for the SMS PCB further reduces the vertical clearance of the sun sensor. With a similar idea as option two, the board fits over the sun sensor but sits high enough that the notch for the connector is not needed; the connector is now below the circuit board. Slightly longer #2-56 screws are used to secure the sun sensor to the board and two separate structures attached to the board are fit into the alignment pins of the sun sensor. This design option is shown in Figure 37.

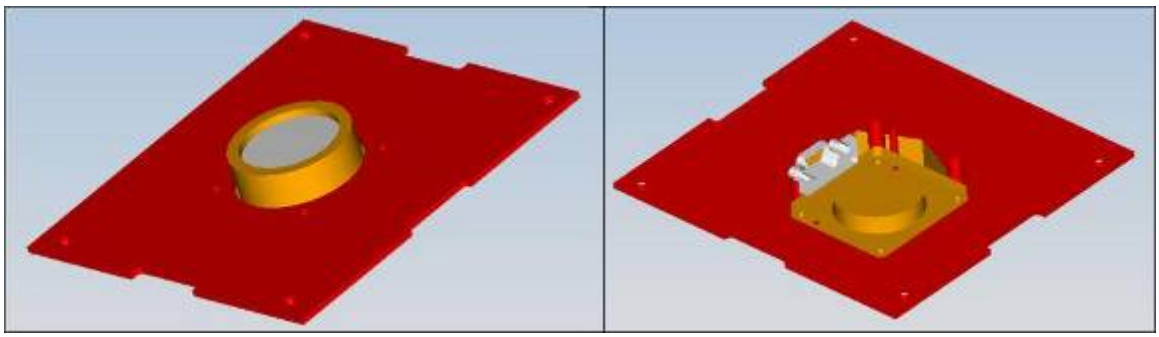

Figure 37 SMS PCB Option Three

The unusable area on the top layer is now reduced to just the cut-out for the circular aperture of the sun sensor. The bottom layer's unusable area for the SMS circuitry is reduced as well but the micro-D connector interference concerns are still present. While the manufacturing of this circuit board would be straightforward, most circuit board manufacturing companies do not have the capability to add additional structures to their boards. With that, the required assembly of the structural components could be time consuming and complicated.

d. Final Design

All three design options were produced in rapid-prototype form using ABS plastic to verify the CAD design. Sun sensor mass models were positioned on each of the prototype boards and placed within the CubeSat structure to verify fit. The design chosen for the SMS circuit board layout was the first option due to its simplicity. Despite the area of the sun sensor's footprint being unusable for circuitry, the bottom and inner layers are still viable options for trace routing. Also, fewer cut-outs, only the screw holes, maintain the most structural strength. Option two did not provide as structurally sound a board and eliminated more surface area for component placement; option three required the circuit board to be too high within the CubeSat structure and added complexity to the manufacturing and assembly; it was probably the least structurally sound of the three options. An image of the chosen PCB design with the sun sensor mounted is shown in Figure 38.

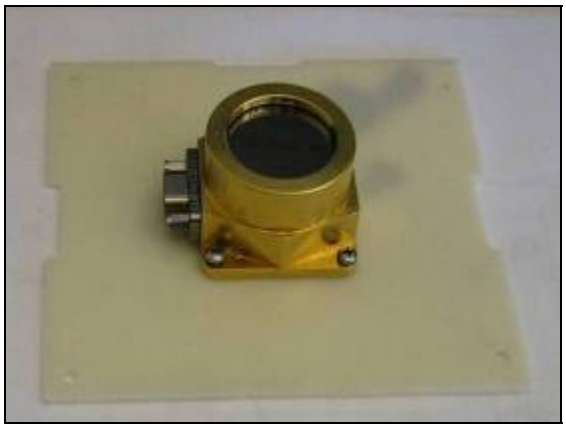

Figure 38 Finalized SMS PCB Mounting Design

Due to the fact that no reference frame had been previously defined for NPS-SCAT, the aforementioned sun sensor reference frame (Figure 34) was also adopted for the satellite. When the sun sensor is placed within the CubeSat, the two coordinate systems are aligned with the exception of an origin offset; the origin of NPS-SCAT's reference frame is the geometric center of satellite. The z-axis is normal to the cover plate assembly of the CubeSat structure; the y-axis is normal to the face with the access ports, pointed from the center of the structure out toward said face; the x-axis is perpendicular to the y- and z-axis faces as in an orthogonal right-handed coordinate system. This coordinate system is shown within the skeletonized NPS-SCAT structure in Figure 39.

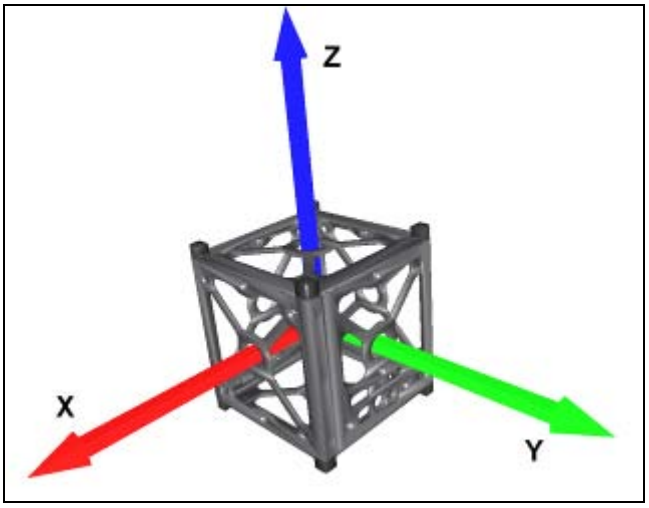

Figure 39 NPS-SCAT Coordinate System Definition

5. SMS Version One

With a finalized configuration for the circuit board structure, the actual circuit board needed to be laid out onto a PCB. SMS V0 could only test one solar cell at a time. The idea with SMS version one (V1) was to have it be able to test two solar cells at the same time, doubling the testing ability of the circuit board. SMS V1 was built to test cells from the ESP V1, already produced and on-hand.

a. Development

The circuit board design program, PCB Artist, was used to develop SMS Version One and all follow-on circuit boards. PCB Artist is a PCB layout CAD program that is offered free through the circuit board manufacturing company Advanced Circuits. It is fairly user-friendly and offers the user the ability to custom design any type of component or circuit board shape. Using the specifications of the CubeSat Kit PC/104 layout, the proper sized circuit board shape was developed, seen previously in Figure 15. A circuit schematic was created, seen in Figure 40 and Figure 41, with two SMS circuits, each with its own MAX680 voltage converter IC. The same components used for SMS V0 were used for the newer version. Several of the required components, specifically resistors, capacitors, and diodes, were selected in surface mount packages. This allowed more room for component placement as the large dual inline package (DIP) components take up considerable space.

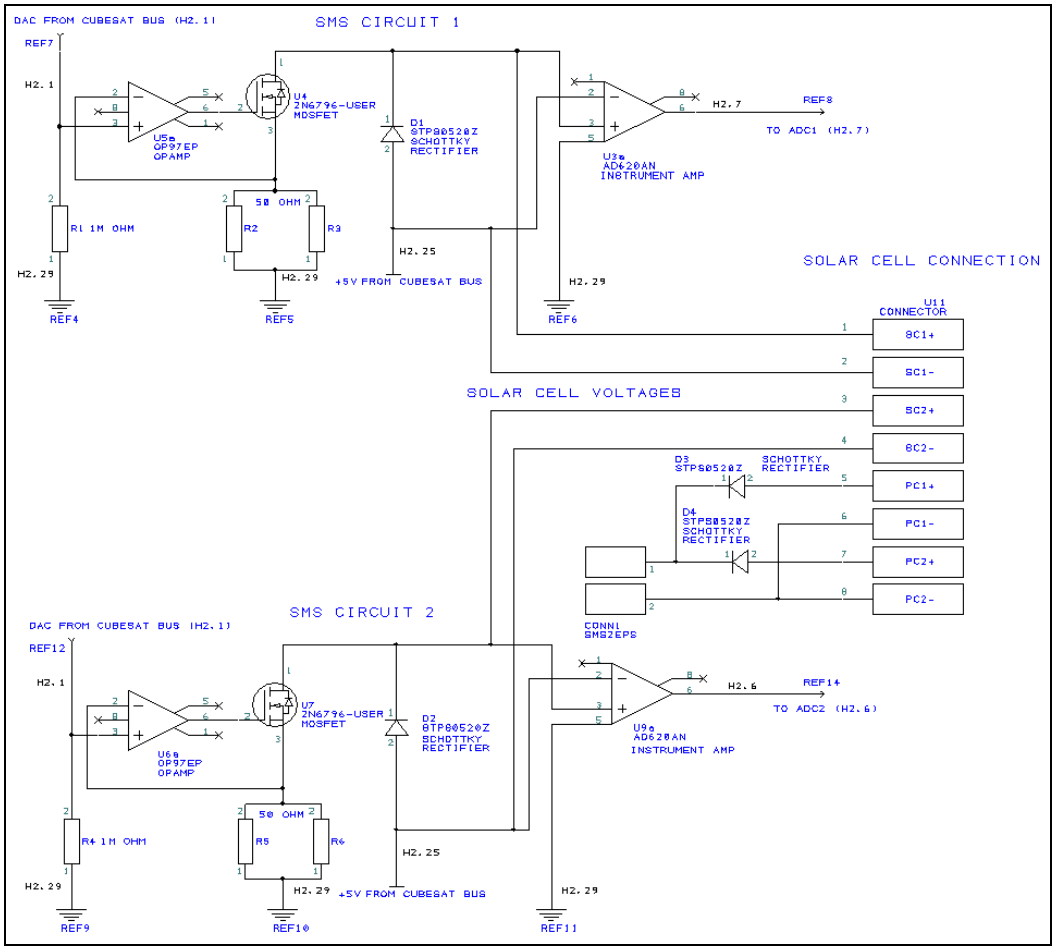

Figure 40 SMS V1 Circuit Schematic (part one of two)

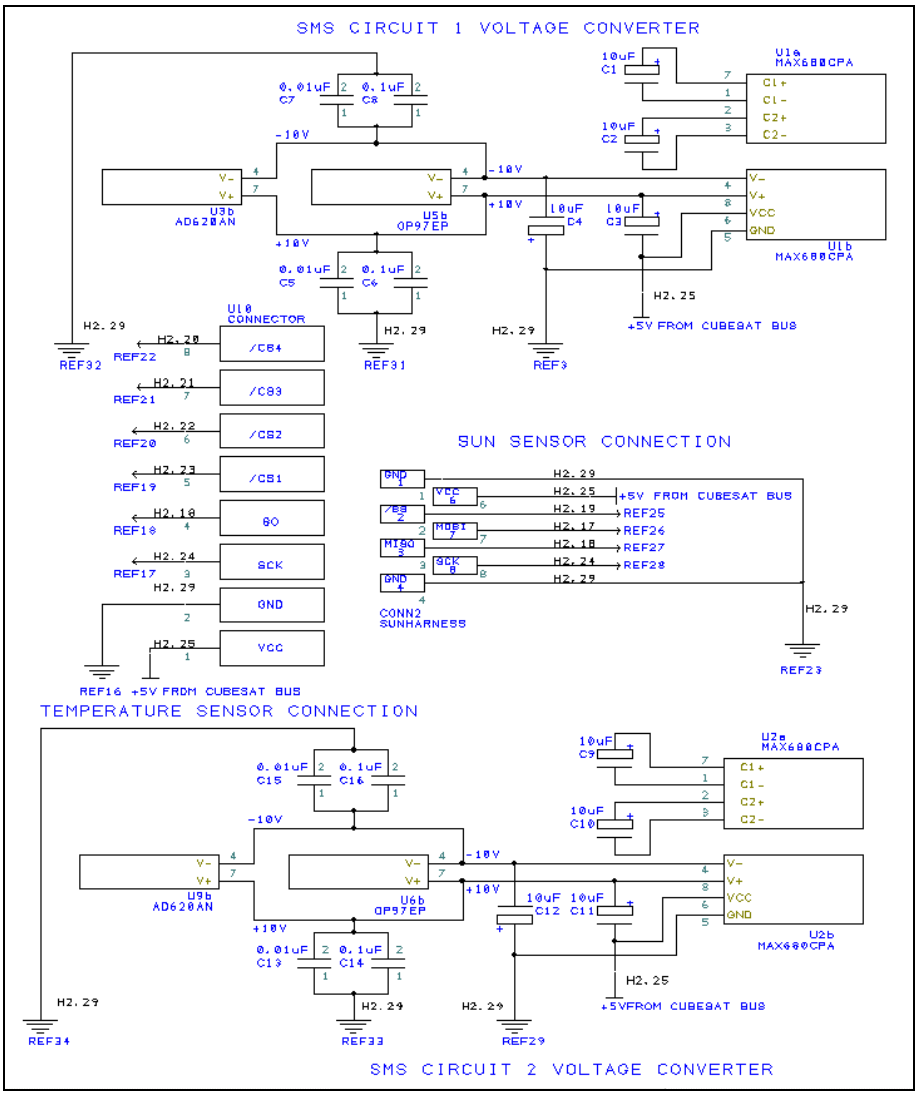

Figure 41 SMS V1 Circuit Schematic (part two of two)

The circuit also had to take into account the required connections external to the circuit board: the sun sensor, temperature sensors on the ESP V1, and selected solar cells to be used for the SMS experiment and for providing power to the EPS. Two solar cells were chosen from the ESP V1 to act as experimental solar cells and be tested by the SMS circuits, labeled SC1 and SC2 in Figure 32. Additionally, two sets of solar cells connected in series on the ESP V1 were picked to act as power cells, labeled PC1 and PC2 in Figure 32. Both of the power solar cell outputs were tied together, with diodes put in place on the positive leads to prevent reverse biasing. No specific connector was used to link the power solar cells to the EPS; the two leads could be

soldered to the component labeled CONN1 on the SMS V1 PCB and connected to the EPS. While this power could be sent to the EPS, the EPS would not be able to use it, unless, as previously mentioned, the voltage exceeded 3.5 V to overcome the minimum voltage requirement of the BCRs. An eight-pin Molex connector was used as the connector to link the SMS V1 and ESP V1 circuit boards. The male connector was located on the SMS V1 PCB. The pin allocation for the connector, describing each board's use of the pins, is shown in Table 7.

Table 7 SMS V1 to ESP V1 Connector Pin Allocation

Pin	Wire Color	SMS Use	ESP Use
1	Red	SC1+	Cell 10+
2	Black	SC1-	Cell 10-
3	Red	SC2+	Cell 13+
4	Black	SC2-	Cell 13-
5	White	PC1+	Cell 1+
6	Black	PC1-	Cell 2-
7	White	PC2+	Cell 20+
8	Black	PC2-	Cell 19-

b. Design Review

Throughout the development cycle of the NPS-SCAT satellite, the need for design reviews repeatedly became apparent. The purpose of a design review is to carefully scrutinize the proposed design, in this case the circuit board schematic and layout, before manufacture. The review by knowledgeable personnel validates the correctness of the design and its implementation. The more thorough the design review, the better the end result. The SSAG Lab Manager, an electrical engineer, proved to be invaluable in this step of the design process and offered many excellent suggestions. For SMS V1, it was decided to create a four layer PCB, with the top and bottom each consisting of a layer, and two inner layers known as power planes. The power plane just below the top layer was set to ground; the layer below the ground plane was set to +5 V. Bypass capacitors were added to all power lines. A bypass capacitor is a small capacitor (0.01 μF - 0.1 μF) connected from the power supply line to ground, "[b]ypassing the power supply at the [power] supply terminals to minimize noise" [64]. They were placed physically as close to the power supply component as possible to reduce signal noise. As

seen in Figure 42, different capacitance values minimize noise at different frequencies. The values chosen for the bypass capacitors were based upon experience with similar systems as recommended by the Lab Manager.

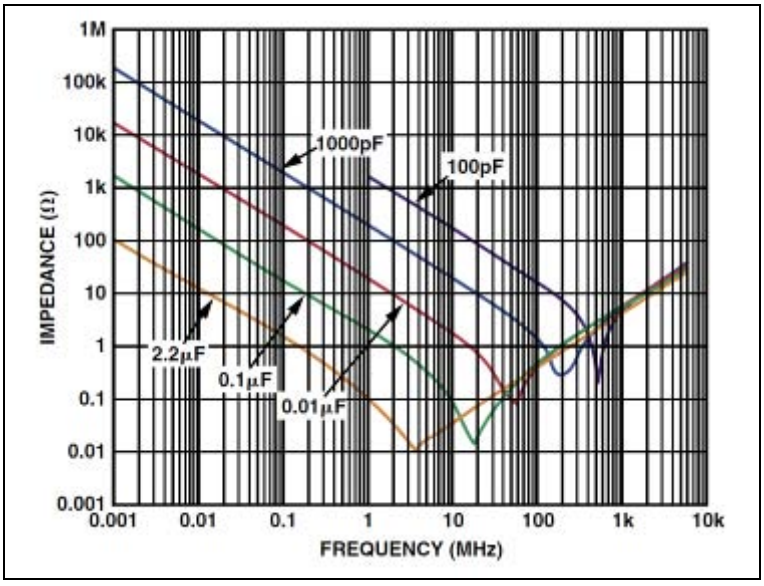

Figure 42 Capacitor Impedance vs. Frequency (From [64])

The trace widths for all of the power lines (±10 V, experimental solar cell, power cell) were widened to 50 mils (0.050 in). The rule for trace width is that the wider the trace, the less resistance and more current capability. The minimum recommended trace width for 0.3 A, the maximum expected current of an ITJ solar cell, is 10 mils (0.010 in) [65]. A 50 mil trace width leaves plenty of margin in the event of something unexpected.

Having two solar cells being tested simultaneously means that there is an additional signal that needed to be read by the FM430 in the form of the second SMS circuit's analog output. The FM430 has multiple ADCs with which it can read analog signals and convert them to digital data. ADC2 was selected to read the data from SMS Circuit Two. With ADC1 reading the data from SMS Circuit One, both experimental solar cells could be tested together when the DAC is ramped from zero to 2.5 V. The list of CSK Bus Connector pins allocated for use by SMS V1 is shown in Table 8.

Table 8 SMS V1 Pin Allocation

Net	Use
H2.1	DAC
H2.6	ADC2
H2.7	ADC1
H2.17	MOSI
H2.18	MISO
H2.19	/SS
H2.20	/SS4
H2.21	/SS3
H2.22	/SS2
H2.23	/SS1
H2.24	SCK
H2.25	+5 V
H2.29	GND

The design review process also helped find a clearance issue between the eight-pin Molex connectors and the CSK Bus Connector in which these components were physically located too close together. This and the aforementioned problems were corrected and the PCB design, as seen in Figure 43, was sent off to be manufactured. To make sense of the circuit board pictures, it is important to understand what the colors represent. The light blue represents copper on the bottom layer while the red represents top layer copper. Silkscreen, a useful tool to label pins and connections on both the top and bottom layers, is shown in dark green for the top layer and purple for the bottom layer. This convention is followed for all circuit boards mentioned in this thesis.

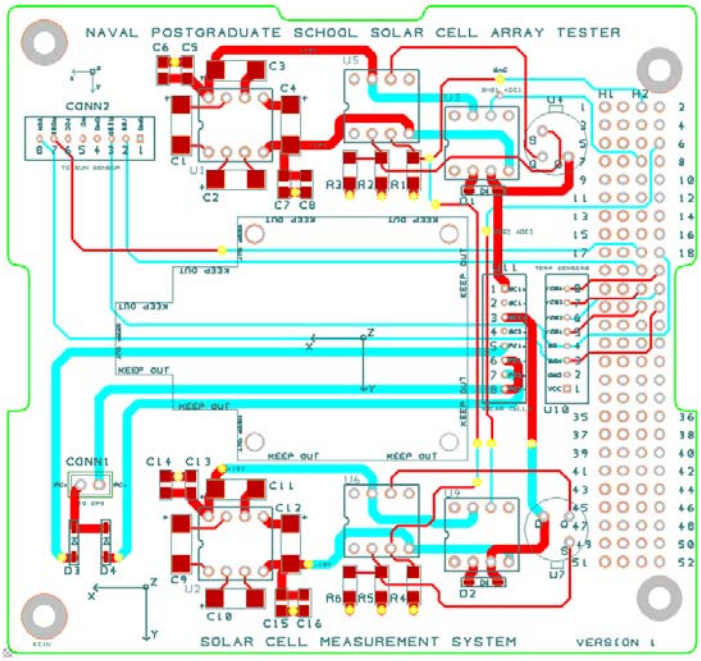

Figure 43 SMS V1 PCB

c. Construction

The construction of the SMS V1 PCB included some surface mount soldering as seen in Figure 44. For the DIP components, sockets were used to allow the individual ICs to be removed if the need arises. Also, the MOSFETs were installed with sockets to allow for easy removal. During component soldering, it was noted that the remaining through-hole components, the three Molex connectors, did not have the proper pin sizing on the circuit board; i.e., the holes were too small. In order for these components to be secured properly to the PCB, a staking compound was used after the pins were soldered to the through-holes. Several pieces of Kapton tape, a polyimide space-grade insulating material manufactured by DuPont, were placed on the back side of the PCB to prevent any connection between the washers, which help secure the sun sensor to the board, and the copper traces. Even though solder mask does cover up all exposed copper traces on the top layer, the Kapton tape adds extra electrical isolation between these items.

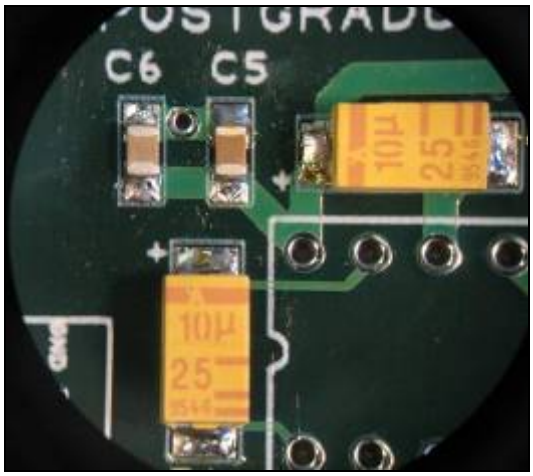

Figure 44 SMS V1 Surface Mount Soldering

During the assembly process, a technique for soldering the smaller package surface mount components was learned. Before placing a component on the pad, a bit of flux was applied using a flux pen. This layer of flux acted as a temporary adhesive, holding the component in place on the pad. Also, the use of a soldering iron set to at least 750°F but not more than 850°F is required for proper application of solder. The use of a microscope greatly aided in the ability to quickly and accurately populate a circuit board and produce a finished SMS V1 board, as seen in Figure 45.

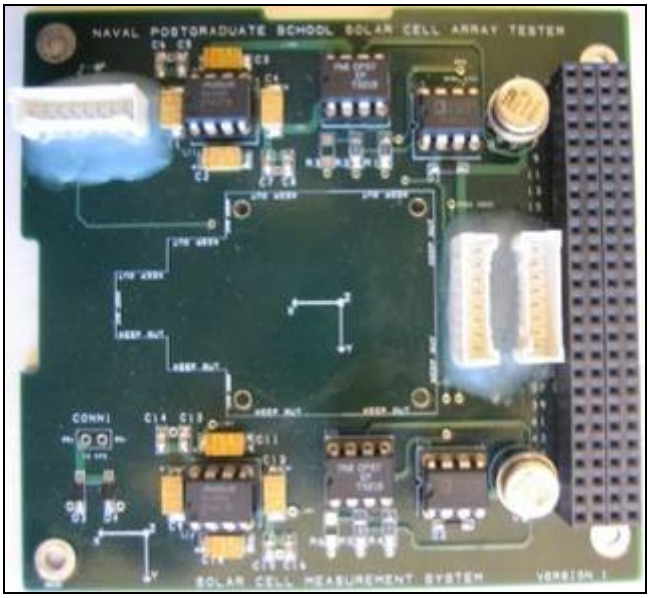

Figure 45 Completed SMS V1 PCB

d. Testing

To ensure complete circuit functionality, a full test of the SMS V1 PCB was conducted. A powered breadboard was used to simulate the CubeSat Kit Bus Connector, providing +5 V, ground, and a DAC input. Three multimeters were used to monitor the DAC voltage, ADC1 voltage, and ADC2 voltage. The CSK Bus Connector on the PCB was connected to the breadboard and multimeters through the use of jumper wires to the relevant signal lines. The zero to +15 V variable voltage supply on the breadboard was used only in the zero to +2.5 V range to simulate the actual DAC capabilities and was connected to the DAC as well as a multimeter. The +5 V and ground connections on the breadboard were connected directly to their respective places on the SMS V1 PCB's CSK Bus Connector.

Figure 46 SMS V1 Functional Test Setup

The test was conducted by first illuminating the ESP V1 with an incandescent lamp that delivered approximately a quarter power of the sun. The zero to +15 V variable voltage connector on the breadboard, simulating the DAC, was slowly changed from zero to 2.5V. At each step in DAC voltage, the voltage displayed on the DAC, ADC1, and ADC2 multimeters was recorded. A sufficient number of points were taken to get a well-defined plot of the solar cell current and voltage for each of the two experimental solar cells. This setup is shown in Figure 46. Figure 47 shows the results of the test, with the top I-V curve of each plot representing the test when SC1 was

illuminated and the bottom plot from when SC2 was being illuminated. Because these solar cells were TASC, the maximum voltage produced was approximately 2.5 V. The maximum current was about 8 mA, demonstrating the fact that the incandescent lamp used to conduct the test does deliver about a quarter sun of illumination. The cell that did not receive full illumination produced significantly less current.

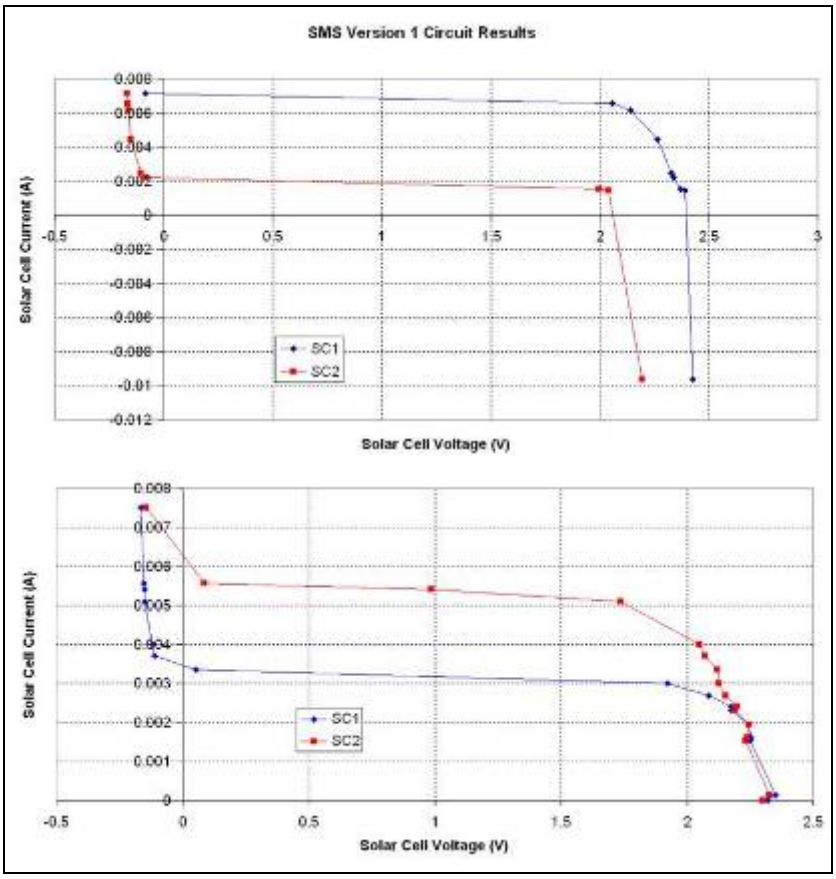

Figure 47 SMS V1 Functional Test Results

In addition to the functional test, the SMS V1 also went under a power consumption test. A multimeter setup for current measurement was placed on the +5 V power supply line in between the SMS V1 PCB and the EPS. This allowed the total current consumption of the SMS V1 to be measured. By changing the states of the SMS V1 (on and off, running tests), the total power consumption for the circuit board was determined. In this manner, the maximum current draw on the 5 V bus by the SMS V1 was about 60 mA, resulting in a maximum power usage of 0.3 W.

6. SMS Version Two

After the successful test of SMS V1, several design changes were desired in order to have a more comprehensive capability to test different types of solar cells. SMS V1 only allowed for a total of two different solar cells to be tested. If a switching mechanism were added, the SMS Version Two (V2) could be able to test more solar cell types all the while keeping a similar configuration and potentially using the solar cells for power while not undergoing a test. Also, as the continuous power consumption of SMS V1 is fairly large, it would be beneficial to have the payload consume minimal power while not conducting a test. SMS V2 was designed to be used with a newer version of the experimental solar panel but is still compatible with the ESP V1.

a. Development

Because the design of the circuit board called for a sizeable leap in complexity from the earlier version, the development for SMS V2 began with component research and selection. The eight-pin sun sensor connector remained the same; however, all of the larger DIP components were found and purchased in the small, space-saving surface mount packages. The same component types for the SMS circuitry as used in the previous version were implemented on SMS V2 except for the MOSFET. The through-hole 2N6796 MOSFET was replaced by the AO4440 MOSFET, which was in a surface mount package. The only through-hole components used were connectors linking to off-board components and subsystems, thereby minimizing the area taken up on two layers of the circuit board. The goal of reducing the component footprints by using surface mount packages was to keep the circuit board layer count to four.

A latching relay was selected as the switching mechanism to meet the requirement of switching the experimental solar cells between the SMS circuitry and the EPS. The Teledyne ER422D-5 magnetic latching relay is a dual pole dual throw (DPDT) relay and takes a +5 V pulsed signal to switch between its two poles. Due to its latching capability, no additional power is necessary to hold the relay in any given position. Internal permanent magnets hold the contact in position until the pulsed signal hits the internal coils, which produce a large enough magnetic field to overcome the permanent

magnet, and the relay switches positions. There are two coils in each relay, designated A and B. The pin-out of the relay when looking at the terminals is shown in the lower part of Figure 48.

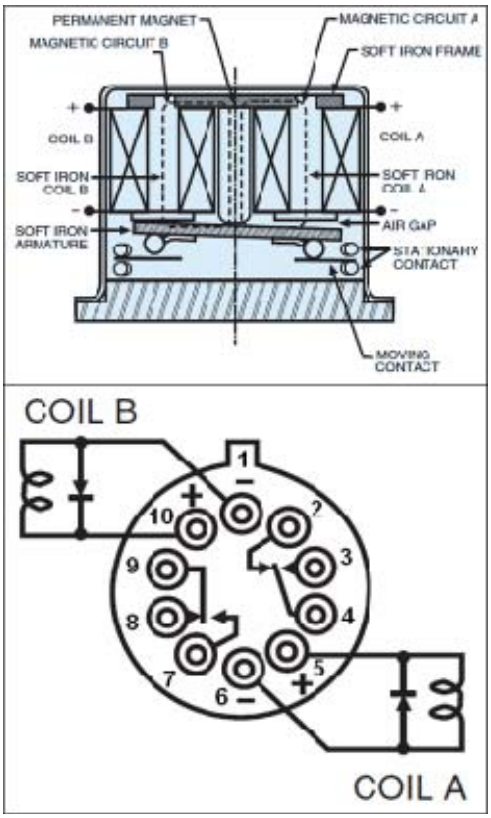

Figure 48 ER422D-5 Relay Configuration (After [66])

Each relay is paired to an experimental solar cell, with the positive and negative terminals of the solar cell attached to the two relay poles. The default position selected for the relays is the position of the contacts when coil A is energized. Four relays were used, which allowed a total of four different experimental solar cells; a fifth was used to act as the on/off switch for the +5 V power supply to the SMS circuitry. When the relays are put into the default position, the experimental solar cells are switched to send power to the EPS and the +5 V power supply for the SMS circuit board is off. The circuit schematic for all five relays is shown in Figure 49.

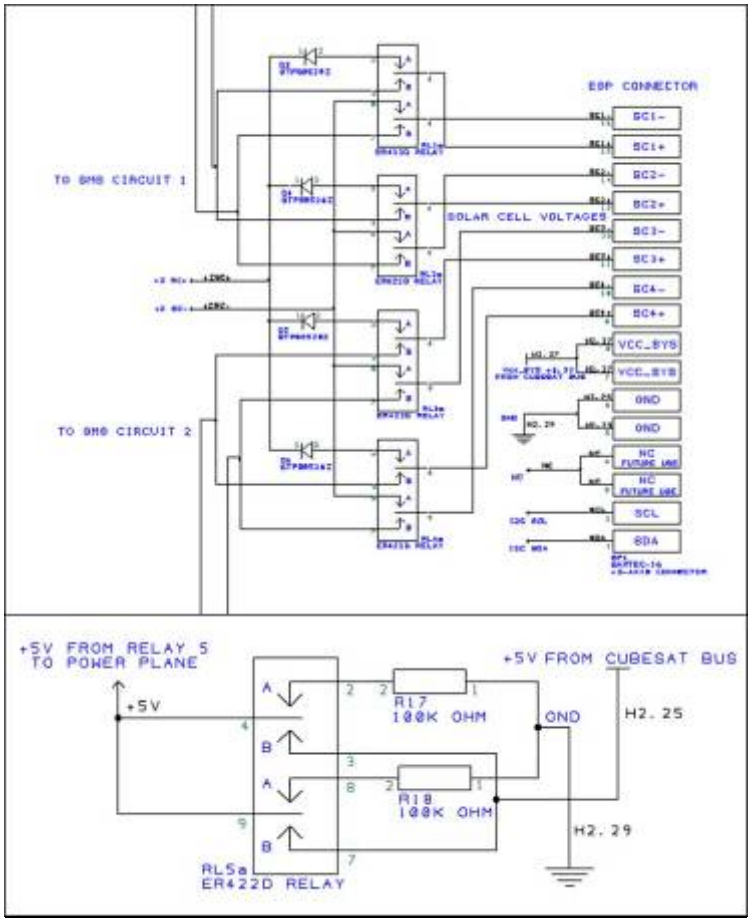

Figure 49 SMS V2 Relay Circuit Schematic

To provide the required +5 V signal to switch the relays, a MAX4427 non-inverting, dual high-speed MOSFET driver was selected, which converts a TTL (transistor-transistor logic) signal from the FM430, which is a lower voltage signal at +3.3 V, into a +5 V signal. To prevent any errant power signals on the SMS circuit board from causing damage to the FM430, an SN74LVC245A bus transceiver with tri-state outputs was selected to act as a buffer between these signals. When the buffer is not enabled, it enters a high impedance state that prevents the transmission of any signals; signals pass through normally when the buffer is enabled. Whenever the FM430 is powered on, the MSP430F1612 microcontroller always initializes its GPIO ports first to an input, which is high impedance, and then to whatever the software commands. Attached to both ends of the buffer gate, in addition to each signal line, is a 20 kΩ resistor that is also attached to ground (a pull-down resistor). This setup keeps the line in

a known state, a logic low, whenever there is not a pulse from the FM430. The MAX4427 relay actuation circuit schematic with buffered command signals for relay one can be seen in Figure 50. The only difference between the relay actuation circuits for the five relays is the power source. Relays one through four receive their +5 V power from the switched power supply provided by relay five. Relay five uses the +5 V provided by the EPS and supplied from the CubeSat Kit Bus Connector.

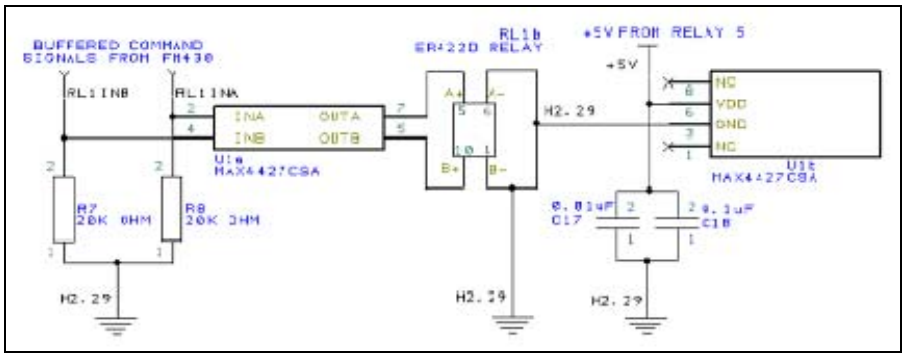

Figure 50 SMS V2 Relay One Actuation Circuit Schematic

Because the payload was being developed before the power solar panels, it was determined that another function of the SMS V2 PCB would be to receive and route temperature data and solar power from all of the solar panels to the appropriate destination. The temperature data is read by the FM430 directly, while the current and voltage data from the power solar cells would be read by the EPS. In addition to having temperature sensors placed on each of the solar panels, one temperature sensor was placed on the SMS V2 PCB. The temperature sensors chosen for the ESP V2 and the remainder of the satellite were different from those used for ESP V1. The MAX6633 digital temperature sensors were chosen, providing the same temperature resolution, with low power consumption, requiring only a +3.3 V power supply, and use an inter-integrated circuit (I^2C) protocol to transmit temperature data. This protocol format reduces the total number of control lines to two. The only required signal lines are the serial data (SDA) and the serial clock (SCL). The I^2C protocol has a 7-bit addressing system to allow communication between devices, with each component possessing a unique address. The MAX6633 temperature sensors have four address pins, allowing up to 16 separate MAX6633 components to be used on the same I^2C bus. There are a total

of 15 temperature sensors on the satellite: each solar panel contains two sensors, located on the inner and outer faces of the panel, except for the experimental solar panel, which has four, one for each experimental solar cell, and one on the SMS V2 PCB. Due to the nature of the I^2C protocol and hardware, the SDA and SCL lines for the bus must be pulled high to +3.3 V. This was accomplished by using two 10 kΩ pull-up resistors on the SMS V2 circuit board. The circuit schematic for the temperature sensor on the SMS V2 circuit board is shown in Figure 51.

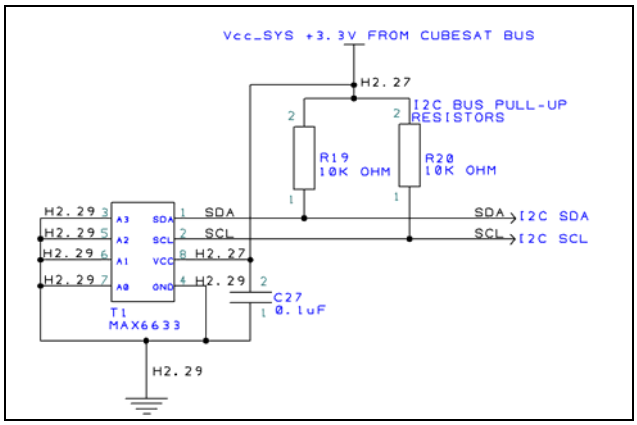

Figure 51 SMS V2 Temperature Sensor Circuit Schematic

Another I^2C component using the same bus as the temperature sensors is the PCA8565 real time clock (RTC). This component "provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal" [67]. Using a 3 V coin cell for its power source, which is also located on the SMS V2 circuit board, this chip is used to timestamp the SMS data during a test. The circuit schematic for the RTC is shown in Figure 52. A table of all the components and their addresses for the primary I^2C bus is shown in Table 9.

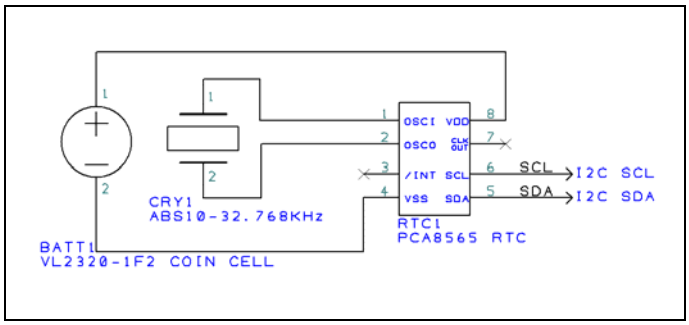

Figure 52 SMS V2 Real Time Clock Circuit Schematic

Table 9 SMS V2 Primary I^2C Bus

Component	Address (Bin)	Address (Hex)	Location
MAX6633 Temperature Sensor 1	01000000	0x40	SMS Printed Circuit Board
MAX6633 Temperature Sensor 2	01000001	0x41	+z-Axis Outer Layer (Experimental Solar Cell 1)
MAX6633 Temperature Sensor 3	01000010	0x42	+z-Axis Outer Layer (Experimental Solar Cell 2)
MAX6633 Temperature Sensor 4	01000011	0x43	+z-Axis Outer Layer (Experimental Solar Cell 3)
MAX6633 Temperature Sensor 5	01000100	0x44	+z-Axis Outer Layer (Experimental Solar Cell 4)
MAX6633 Temperature Sensor 6	01000101	0x45	+y-Axis Outer Layer
MAX6633 Temperature Sensor 7	01000110	0x46	+y-Axis Inner Layer
MAX6633 Temperature Sensor 8	01000111	0x47	+x-Axis Outer Layer
MAX6633 Temperature Sensor 9	01001000	0x48	+x-Axis Inner Layer
MAX6633 Temperature Sensor 10	01001001	0x49	-x-Axis Outer Layer
MAX6633 Temperature Sensor 11	01001010	0x4A	-x-Axis Inner Layer
MAX6633 Temperature Sensor 12	01001011	0x4B	-y-Axis Outer Layer
MAX6633 Temperature Sensor 13	01001100	0x4C	-y-Axis Inner Layer
MAX6633 Temperature Sensor 14	01001101	0x4D	-z-Axis Outer Layer
MAX6633 Temperature Sensor 15	01001110	0x4E	-z-Axis Inner Layer
PCA8565 Real Time Clock	01010001	0x51	SMS Printed Circuit Board

Two buffers, with a similar function as the one used for the relay control signals, were used to isolate the SPI and I^2C buses from accidentally causing harm to the FM430 GPIO pins to which they are connected. The SPI bus buffer was the SN74LVC126A chip and it isolates the four SPI control lines used to communicate with the sun sensor. The PCA9517 IC is the buffer for the I^2C bus. Both of these components enter a high impedance mode when they are not enabled. The enable pin, which has been designed to be active high for all three buffer components, is attached to the same control signal line from the FM430. The schematics for all three buffer gates are shown below in Figure 53.

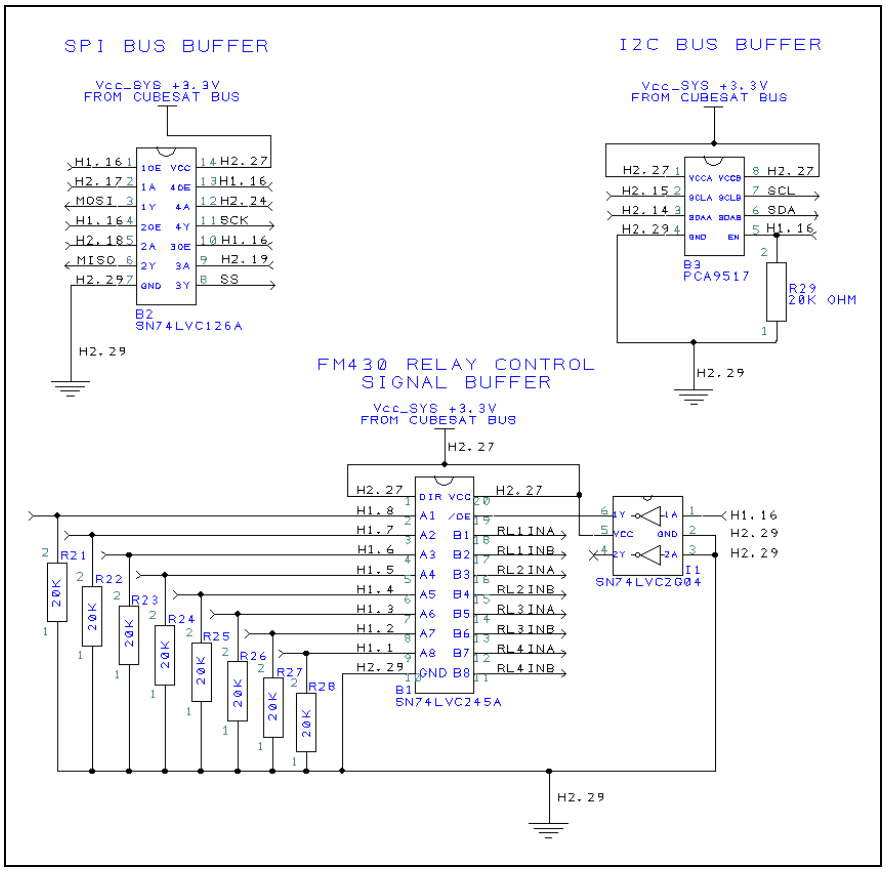

Figure 53 SMS V2 Logic Signal Buffer Gate Circuit Schematic

To connect all six solar panels to the SMS V2 PCB, a compact, high-density Samtec connector was selected the carry the necessary power and control lines between the circuit boards. The five power solar panels (±x, ±y, and –z) all share the same type of Samtec 10-pin connector, FTSH-105-L-D-K(-RA). The connector PCB footprint (looking at the circuit board) and pin functions are shown in Figure 54 and Table 10, respectively.

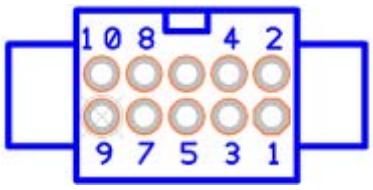

Figure 54 SMS V2 to Solar Panel Connector

Table 10 SMS V2 to Solar Panel Connector Pin Allocation

Pin	Function
1	SDA
2	SCL
3	GND
4	GND
5	+3.3 V
6	+3.3 V
7	Solar Cell -
8	Solar Cell -
9	Solar Cell +
10	Solar Cell +

The newest version of the experimental solar panel, ESP V2, has a connector that was designed to interface the temperature sensors and also connect the four experimental solar cells to the SMS V2 circuit board. This connector, the FTSH-108-01-L-D-K(-RA), is also manufactured by Samtec and has a keying shroud, as does the previously mentioned solar panel connector, to allow for a unique mating orientation. The connector PCB footprint and pin functions are shown in Figure 55 and Table 11, respectively.

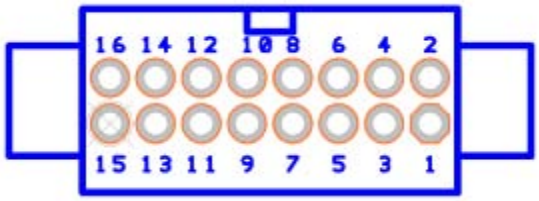

Figure 55 SMS V2 to ESP V2 Connector

Table 11 SMS V2 to ESP V2 Connector Pin Allocation

Pin	Function
1	SDA
2	SCL
3	NC
4	NC
5	GND
6	GND
7	+3.3 V
8	+3.3 V
9	Solar Cell 4+
10	Solar Cell 4-
11	Solar Cell 3+
12	Solar Cell 3-
13	Solar Cell 2+
14	Solar Cell 2-
15	Solar Cell 1+
16	Solar Cell 1-

The Clyde Space EPS has three six-pin connectors that are used to accept the solar panel power. Each of these connectors, the Hirose DF13-6P-1.25DSA, represents one of the satellite's axes (x, y, and z) and has pins for the positive and negative axis face solar panels. The SMS V2 PCB was designed so that the same connector will be used. The solar cells on each of the solar panels produce current that flows from the solar panel to the SMS V2 circuit board and then finally to the EPS. The functions of the connector pins are shown in Table 12.

Having the electrical power being routed through the SMS circuit board came about because of the choice of temperature sensors. The Clyde Space EPS is designed to use a type of temperature sensor other than the MAX6633 components chosen for use on NPS-SCAT. The NC pins on the Hirose connector are where the Clyde Space EPS would get temperature telemetry if one were using the Clyde Space solar panels. In order to limit the amount of connectors required to be placed on the solar panels, a single connector was chosen to link the NPS solar panels to the rest of the satellite. The final design resulted in the SMS V2 PCB functioning as the solar panel hub because it was not a COTS component, and, unlike the Clyde Space EPS, could be modified as needed.

Table 12 SMS V2 to EPS Connector Pin Allocation

Pin	Function
1	+Solar Cell+
2	+Solar Cell-
3	NC
4	-Solar Cell+
5	-Solar Cell-
6	NC

b. Design Review

The SMS V2 circuit board went through multiple design reviews due to the increase in complexity. After each stage of integrating a new component into the circuit and component layout, the changes were thoroughly reviewed. It was suggested to change the power planes to reflect the power usage of the components. What was previously a continuous power plane used for the +5 V power source, tied directly to the CubeSat Kit Bus in SMS V1, now takes into consideration that this power is switched by one of the latching relays. A split power plane was created on the third layer of the PCB to allow multiple power voltages on the layer. This is represented by Figure 56. The colors were added to aid in easily distinguishing the different planes. The blue plane is the +5 V provided by the CSK bus, which is always on when the satellite is powered up. The red plane indicates the switched +5 V, controlled by relay five. The green plane is the +3.3 V provided by the CSK bus, which is also always on when NPS-SCAT is powered.

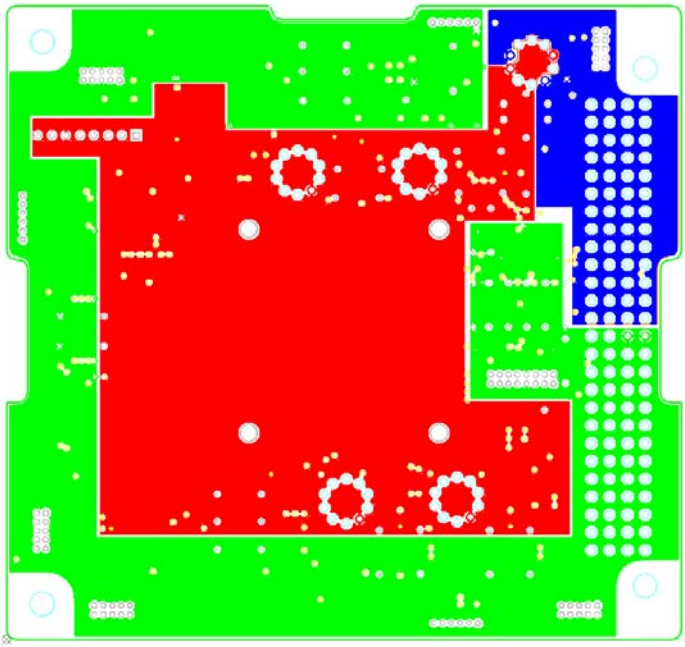

Figure 56 SMS V2 PCB Layer Three

Other issues that came up during the design review were addressed. The hole sizes for the through-hole components were verified to be large enough for the component pins. For the +5 V switching relay, the configuration seen in the lower part of Figure 49 was developed to prevent having an isolated, floating voltage when the SMS circuit board was powered off. Connecting the SMS +5 V plane through a 100 kΩ resistor to ground allows any residual current to be discharged when the power is turned off. The widths of all the traces were sized to accommodate the amount of current they are expected to carry, calculated using a PCB trace width calculator based on the ANSI (American National Standards Institute) standards [68]. The Samtec and Hirose connectors are 30 AWG (American Wire Gauge). The maximum expected current from the solar cells is no more than 0.5 A. The current carrying capacity of a 30 AWG wire is 0.86 A which works out to a 33 mil trace width; 0.50 A requires a trace that is 15 mil wide. The trace width for power signals was chosen to be 25 mil, permitting a maximum of 0.70 A of current. Signal lines were set at a 10 mil trace width. In order to meet the

design rule check within the PCB Artist program, all via sizes were changed to 15 mil hole sizes and a 25 mil width. The finalized PCB schematic sent out for manufacturing is shown in Figure 57.

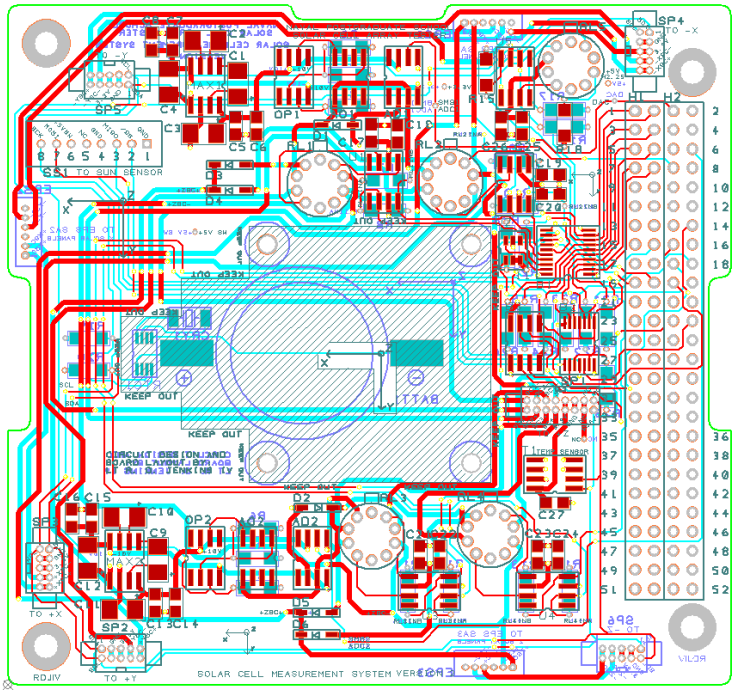

Figure 57 SMS V2 PCB

c. Construction

The SMS V2 PCB was populated in a similar manner as the previous version. Careful attention was paid when soldering the surface mount components once the plastic connecters had been installed to avoid accidentally melting the plastic. Sockets were installed in place of actually soldering the relays to the circuit board. The populated board, minus the CSK Bus Connector, is shown in Figure 58.

Figure 58 Construction of SMS V2 PCB

d. Testing

Upon initial testing, it was immediately apparent there were some errors in the design of the circuit board. Simple continuity tests verified the +5 V power plane was not attached to the two pins on the CubeSat Kit Bus Connector. This error prevented the +5 V from being distributed to the entire circuit board. To correct this, a jumper wire was soldered between the two pins on the CSK Bus Connector (H2.25 and H2.26) and a via that was connected to the +5 V power plane.

When the I^2C components were tested, they did not respond properly to the FM430 commands. The two control lines, SDA and SCL, were found to not be pulled up as required by the I^2C protocol in the segment of traces between the CSK Bus Connector and the PCA9517 buffer chip. This was corrected by adding two additional pull-up resistors to the I^2C lines, seen as the white wire connections in Figure 59.

During the testing to verify satisfactory communication with the sun sensor, it was discovered that the SPI bus was not functioning properly. After verifying the connections, the directionality of the MISO pin to the SPI buffer chip was not correct. The SN74LVC126A buffer chip only allows signals to pass in one direction, preventing bidirectional travel like the I^2C buffer IC. The inputs of pin six and pin five on the buffer needed to be swapped, changing the sun sensor MISO control line with the CSK Bus

Connector pin H2.18. Because the MISO control line sends data from the slave component, in this case the sun sensor, to the master, the FM430, the initial design had the data flowing backwards, which prevented proper communications. This was fixed by cutting the two incorrect traces on the circuit board and making the correct connections using wire jumpers, also seen in Figure 59

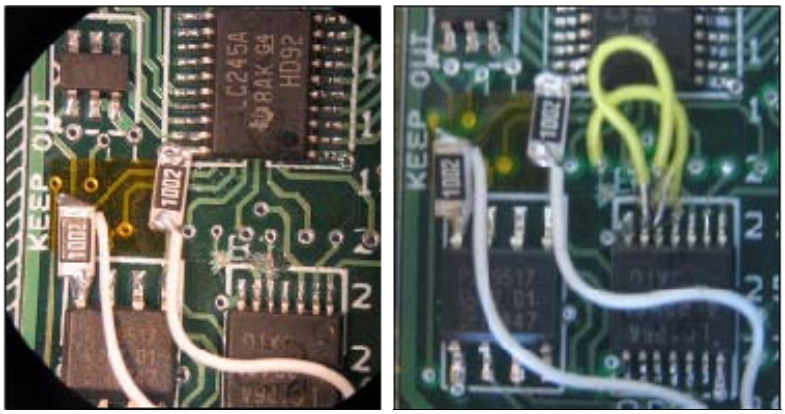

Figure 59 SMS V2 PCB Corrections

Once the I^2C bus was fixed, the real time clock was tested and set to the correct time and date. However, the component did not output a consistent stream of correct data. Upon investigation of the hardware, it was noticed the negative terminals on the real time clock and coin cell were not connected to the satellite's common ground. Another jumper wire was used to make this corrective connection. This is shown as the yellow wire in the right image of Figure 60.

Figure 60 Completed SMS V2 PCB with Sun Sensor (front and back)

A Samtec connector was modified to link the SMS V2 PCB to the ESP V1 circuit board, which provided the experimental solar cells for testing. An additional solar cell was chosen to be used from the ESP V1 in addition to the previous two cells used (SC1 and SC2). Designated SC4, this solar cell can be seen in the labeled ESP V1 schematic in Figure 32. The modified connector consisted of wires soldered to the correct pins on the male Samtec connector, which mates with the female Samtec ribbon cable connector, seen in Figure 61.

Figure 61 SMS V2 to ESP V1 Connector

The SMS V2 circuitry was validated in the same manner as the SMS V1, using a powered protoboard to provide the +5 V power source and variable voltage DAC. With the ESP V1 illuminated using the same incandescent lamp, three multimeters were used to read off the DAC, ADC1, and ADC2 voltages while the DAC was ramped from 0 to 2.5V to produce many data points. The resulting I-V curves from SC2 and SC4 are shown in Figure 62.

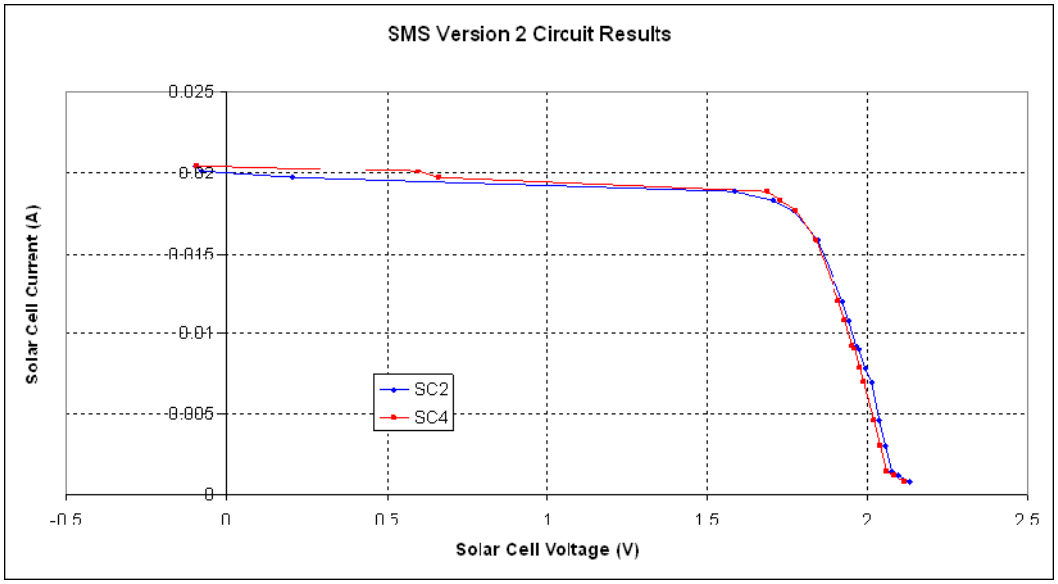

Figure 62 SMS V2 Functional Test Results

7. ESP Version Two

The second version of the experimental solar panel, ESP V2, was developed to act as the +z-axis solar panel and replace the older ESP V1, which was originally built for the prototype. The ESP V2 will hold four individual solar cells that can be tested by the circuitry on versions two and three of the SMS printed circuit board.

a. Development

Initially, the overall structure of the circuit board was designed based upon the previous version of the ESP. The panel has a hole cut in the center of the board to accommodate the sun sensor's aperture. This hole decreases the overall area that can be used for solar cell and component placement. Other objects to be avoided included the solar panel clips in the corners, which hold the ESP to the cover plate assembly. Each solar cell will have its own dedicated, MAX6633 temperature sensor. Given the remaining space available for solar cells, an area was made to maximize the solar cell size, seen in Figure 63. The dimensions of this initial solar cell shape are shown in Figure 64, with the dimensions in millimeters.

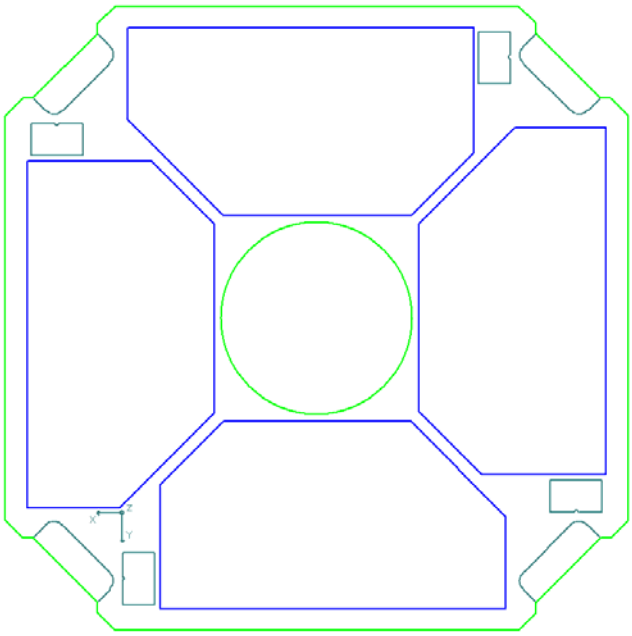

Figure 63 ESP V2 PCB Initial Design

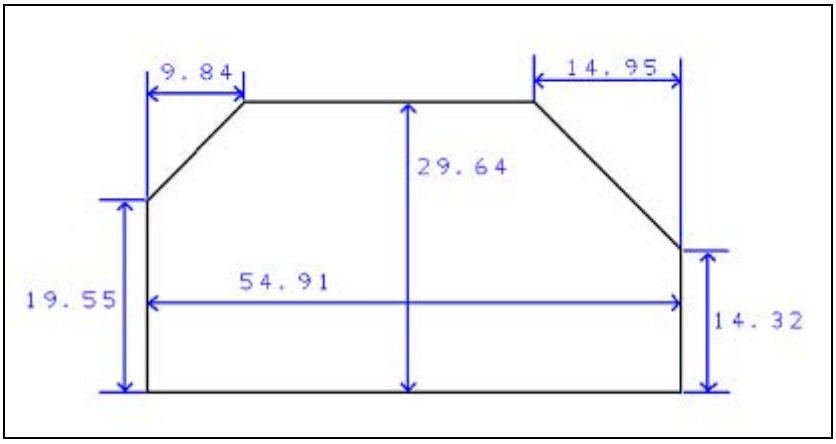

Figure 64 Initial Experimental Solar Cell Dimensions

Once the components were added, it became clear that the area of one of the solar cells needed to be reduced to fit the 16-pin Samtec connector. As no specific experimental solar cells were identified at the time of design, it was decided that one of the experimental solar cells would be a TASC. Several CubeSats have flown these solar cells but there has been no data produced on how they degrade over time. This decision resulted in a reduction in the area required for one of the solar cells, allowing for

placement of the ESP to SMS Samtec connector. The remaining three test solar cells could utilize the original footprint on the circuit board.

Several solar cells were researched to determine if they would be a good candidate as experimental solar cells. Because a TASC was chosen for SC2, a solar cell with a similar current output was desired for SC1 to be compatible with the SMS circuitry. For testing purposes, another TASC was chosen for SC1. The SC3 and SC4 slots were to be filled with single junction silicon solar cells, readily on-hand within the SSAG lab. The design of the ESP V2 maintains the capability to put larger sized solar cells despite that other sized cells were chosen. The size of the available area on the ESP V2, even though it is larger than the TASCs, is too small to fit solar cells that are currently being manufactured. As a solution to this problem, the large area solar cells need to be cut down to fit onto the ESP V2. Several companies have been identified that offer solar cell dicing services which will provide solar cells that maximize the available area on the solar panel. The design using TASC and silicon cells for the experimental cells will be the primary focus for this version of the experimental solar panel.

The circuit schematic for the ESP V2 circuit board is very straightforward, with four temperature sensors and one large 16-pin connector that is directly connected to the four experimental solar cells and the required housekeeping signals. Each of the temperature sensors has a 0.1 μF bypass capacitor to minimize the noise that may be received from the CSK 3.3 V power source. These sensors were addressed in accordance with Table 9. The ESP V2 circuit schematic is shown in Figure 65.

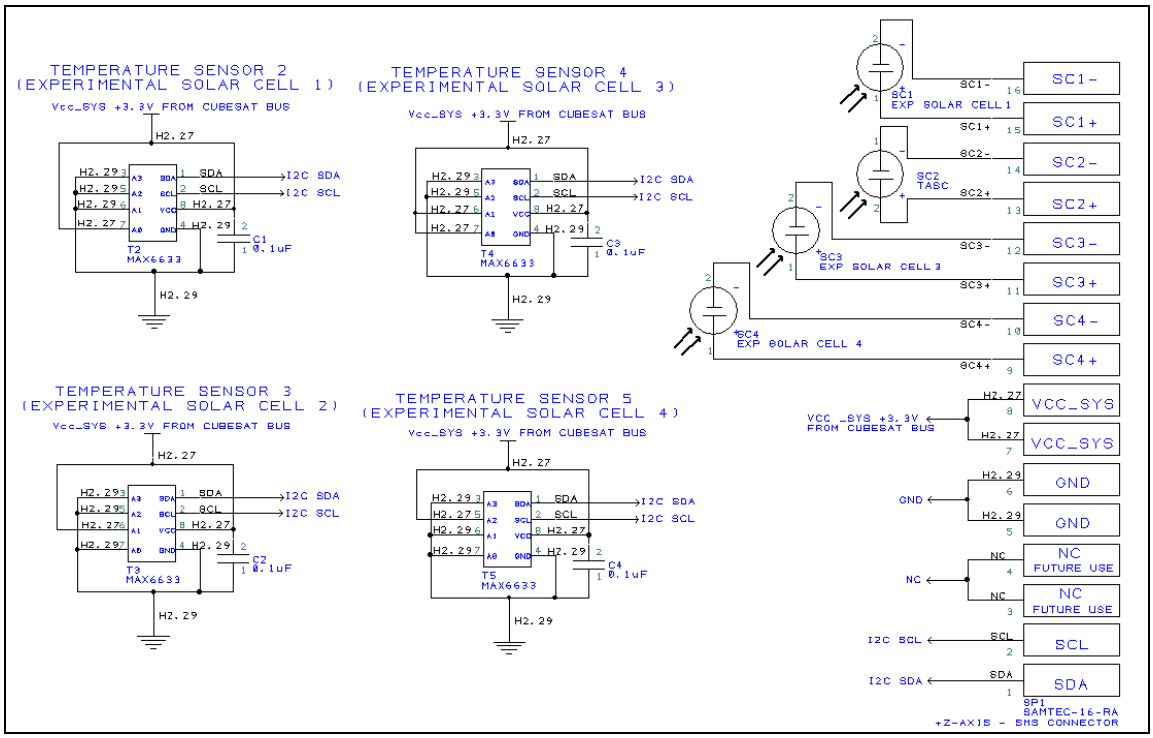

Figure 65 ESP V2 Circuit Schematic

b. Design Review

The design for the EPS V2 included some minor changes as recommended by the reviewers. A silkscreen outline of the TASC was created for the four cells so that in the event all solar cells are chosen to be TASC, it will be easy to properly position them. The bypass capacitors for the temperature sensors were moved to the bottom. A silkscreen outline of the cutouts required for the cover plate assembly was also added. As the final experimental solar cells had not been selected, extra soldering contacts for the solar cells were added to provide flexibility when the time comes to permanently affix the chosen experimental cells.

Also, the circuit board was selected to be a six layer board to prevent any traces from being exposed on the top or bottom layers. If traces were on the top layer, the solar cells would have to be mounted on an uneven surface, whereas if there were traces on the bottom, the metal cover plate assembly might interfere with the signals. With a six-layer board, all traces remained internal to the board, as shown by the brown and blue traces on layers four and five, respectively, in Figure 66.

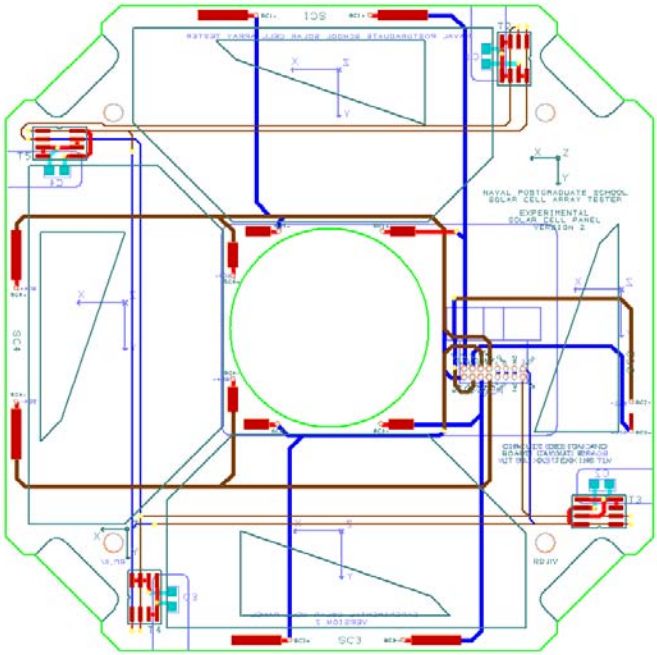

Figure 66 ESP V2 PCB

c. Construction

Upon receipt of the manufactured circuit board, the temperature sensors, capacitors, and the Samtec connector were soldered to their respective pads. To fix the solar cells to the ESP V2, a special technique was required. A contact must first be soldered to the back side of the solar cell. When soldering to the back of the solar cell, one should take care to minimize the amount of solder to prevent a bump that could cause cracking when attaching the cell to the circuit board. The back side of most solar cells is the positive terminal. The negative terminal is generally located on the front. A picture representing procedure for soldering a contact to the positive terminal of the TASC is shown in Figure 67.

Figure 67 TASC Soldering Technique

An adhesive tape called NuSil CV4-1161-5 was used to securely hold the solar cells to the solar panel. The NuSil is a double-sided Kapton tape that can be cut into any shape. A visual representation of the steps taken to place a TASC onto the ESP V2 is shown in Figure 68. Note the cutout made for the soldered contact in the upper left image. The negative terminal on the solar cell was connected to the PCB using a small piece of wire, shown in the lower right image.

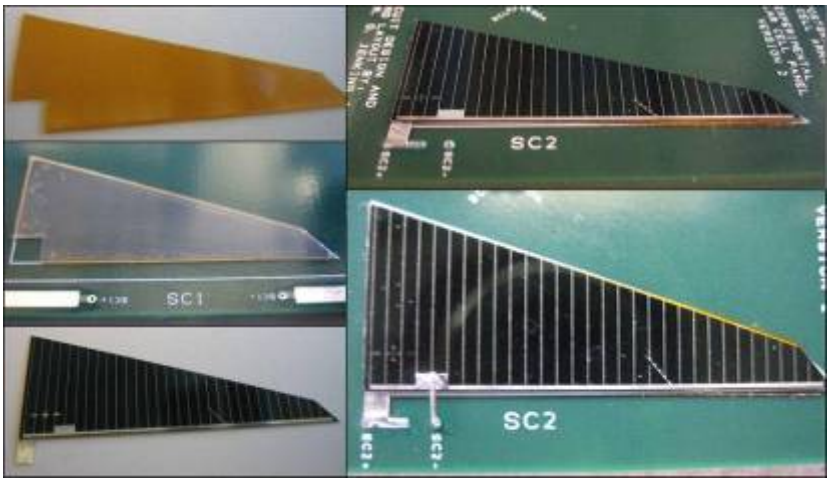

Figure 68 TASC Placement on ESP V2

For the silicon solar cells, the contacts on the circuit board were not optimally positioned. The positive terminals still used the same technique as described above for the TASC, using the pre-soldered contact. To make the connections between the solar cell negative terminals and the board, jumper wires were required. The ESP V2 populated with TASC and silicon solar cells is shown below in Figure 69.

Figure 69 Completed ESP V2 PCB

d. Testing

The ESP V2 was tested for connectivity to verify the soldering workmanship. Full testing, requiring the SMS V3 circuit board, was conducted and is described in the next section.

8. SMS Version Three

A revision of the SMS V2 circuit board was made but with minimal changes. The only alterations made were to correct the errors in SMS V2 already mentioned and also add a slight bit of flexibility for the real-time clock power supply.

a. Development

First, the +5 V power plane was connected to the two power-providing pins on the CubeSat Kit Bus Connector (H2.25 and H2.26). The SPI bus buffer control line that was incorrectly setup on the SMS V2 was fixed to reflect the proper signal flow direction. For the I^2C bus buffer, two 10 kΩ pull-up resistors were added to the CSK Bus Connector side. These two changes can be seen in the updated circuit schematic of Figure 70.

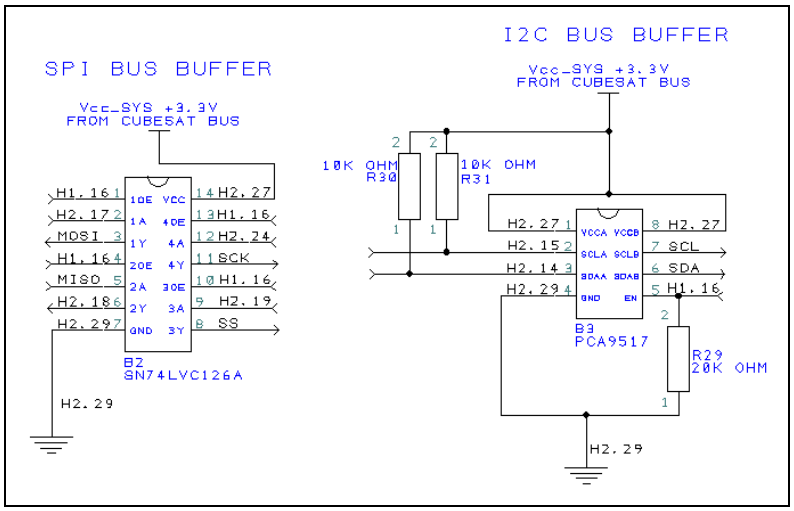

Figure 70 SMS V3 SPI and I^2C Buffer Gate Circuit Schematic

For the real-time clock setup, the negative terminals of the RTC chip and the coin cell were connected to the common ground of the satellite. Also added to this circuit was the ability to power the RTC using the satellite's +3.3 V power source by fitting a 0 Ω resistor for R100. This was added because a future launch provider might prohibit the use of a lithium-ion cell within the NPS-SCAT satellite. The revised circuit schematic is shown in Figure 71.

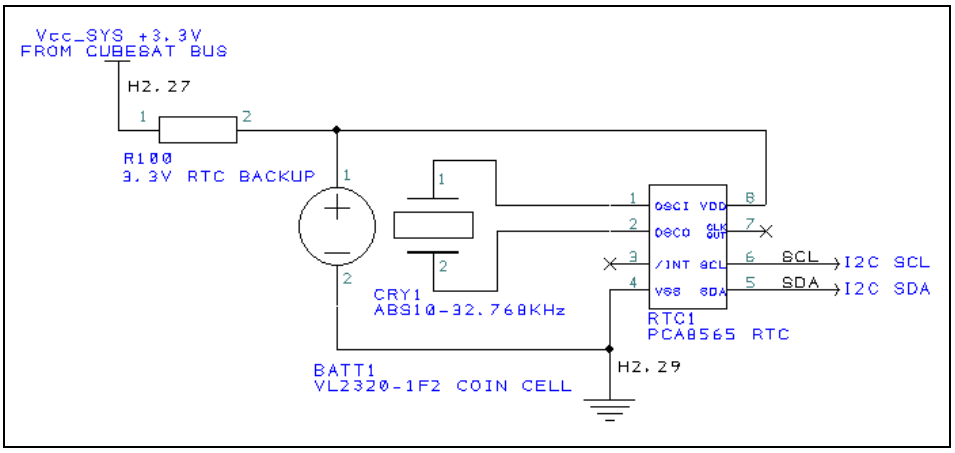

Figure 71 SMS V3 Real Time Clock Circuit Schematic

b. Design Review

Due to the minimal changes between SMS V2 and SMS V3, the design review process went fairly quickly. All of the changes were reviewed and implemented. The finalized circuit board layout is shown in Figure 72.

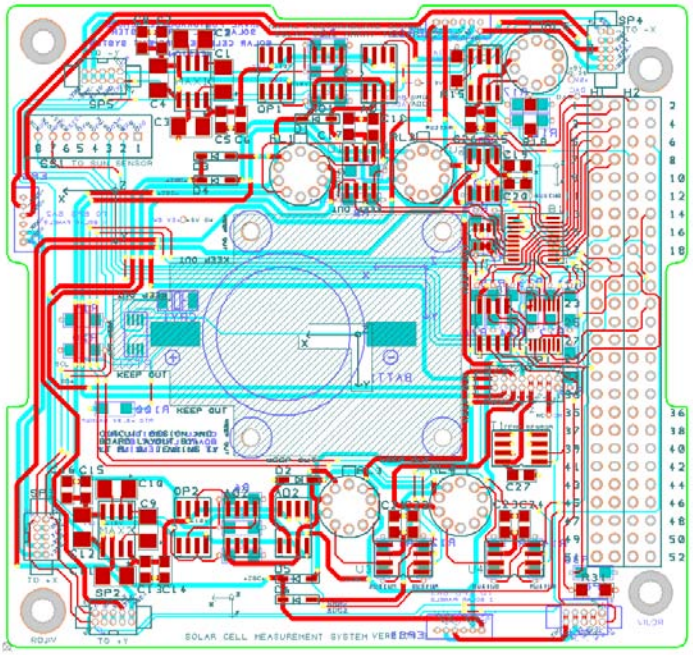

Figure 72 SMS V3 PCB

c. Construction

The assembly process for SMS V3 was straightforward. The five relays were permanently soldered directly to the circuit board for this version. The relays were kept at a maximum height of 7 mm above the circuit board to prevent an interference with the sun sensor. The fully populated circuit board is shown in Figure 73.

Figure 73 Completed SMS V3 PCB (front and back)

d. Testing

The SMS V3 circuit board was tested with the ESP V2 PCB. Using a similar test setup as used for SMS V1 and SMS V2, the procedure was repeated for all four experimental solar cells. The CubeSat, replacing the powered protoboard, provided the +5 V, +3.3 V, and the command signals required to enable the buffers and actuate the relays. Three multimeters were used to record the voltage steps for each point of the DAC, ADC1, and ADC2 as shown in Figure 74. The four I-V curves produced by the SMS V3 testing were plotted together on the same graph, shown in Figure 75. The orange and blue lines are from the two UTJ TASC, which each produce about 2.5 V. The two silicon solar cells, shown in green and red, produced approximately 0.5 V, as expected.

Figure 74 SMS V3 Functional Test Setup

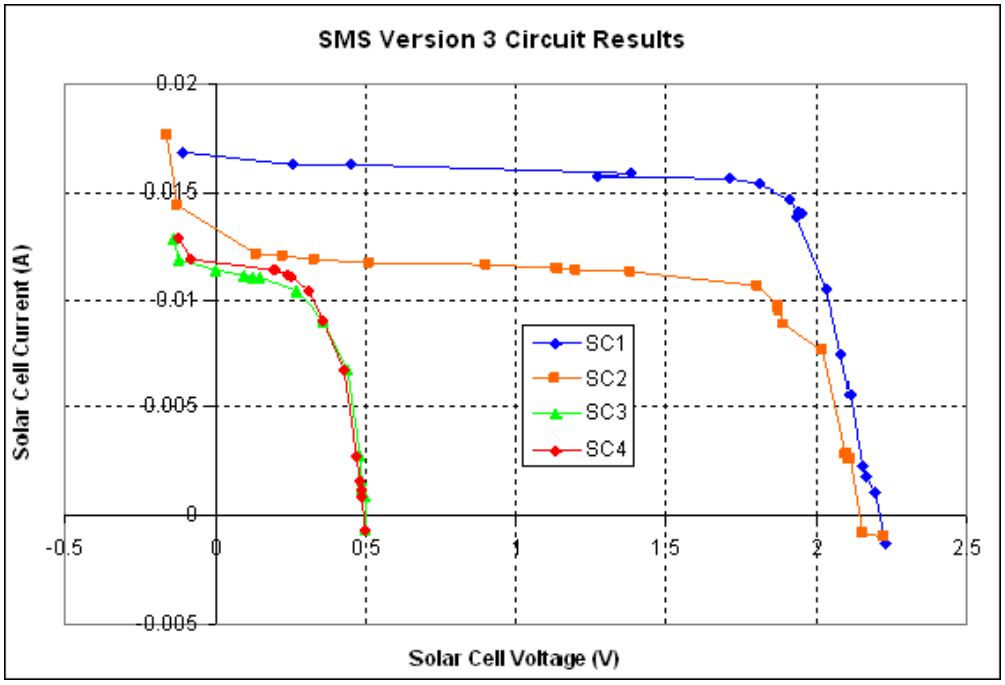

Figure 75 SMS V3 Functional Test Results

A power consumption test for the SMS V3 circuit board was conducted to determine the total amount of power used by the SMS subsystem. The SMS V3 PCB was completely removed from the NPS-SCAT stack and all necessary connections to the SMS board were made between the two using insulated wires. Two ammeters were placed in between the +5 V and +3.3 V power supply lines to measure the current. Two voltmeters were used to monitor the voltage of these two buses. The satellite was then powered on and conducted a series of tests with the SMS circuit board to include

gathering I-V curves, sun angle from the sun sensor, and switching relays to test the different experimental solar cells. When each cycle was over, the SMS was then powered off using the relay to control the +5 V power supply (relay five). The resulting two figures (Figure 76 and Figure 77) show the +5 V bus current and voltage during the test, consisting of a total of eleven cycles.

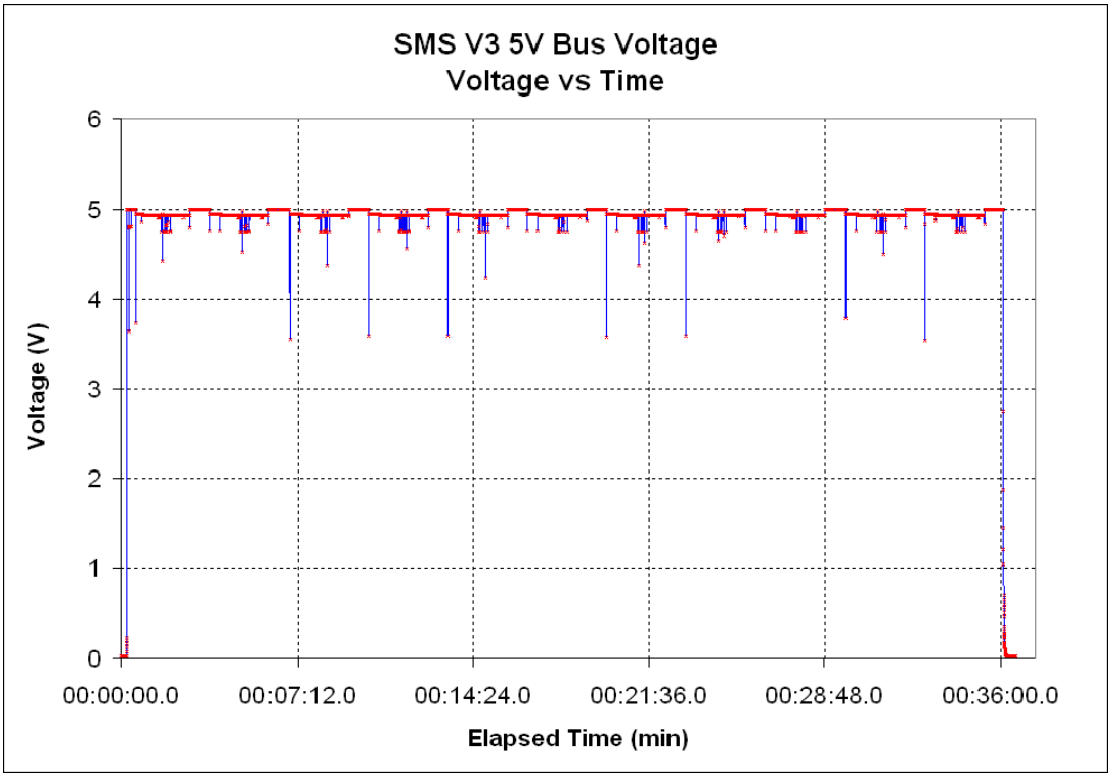

Figure 76 SMS V3 Power Consumption Test Results: 5 V Bus Voltage

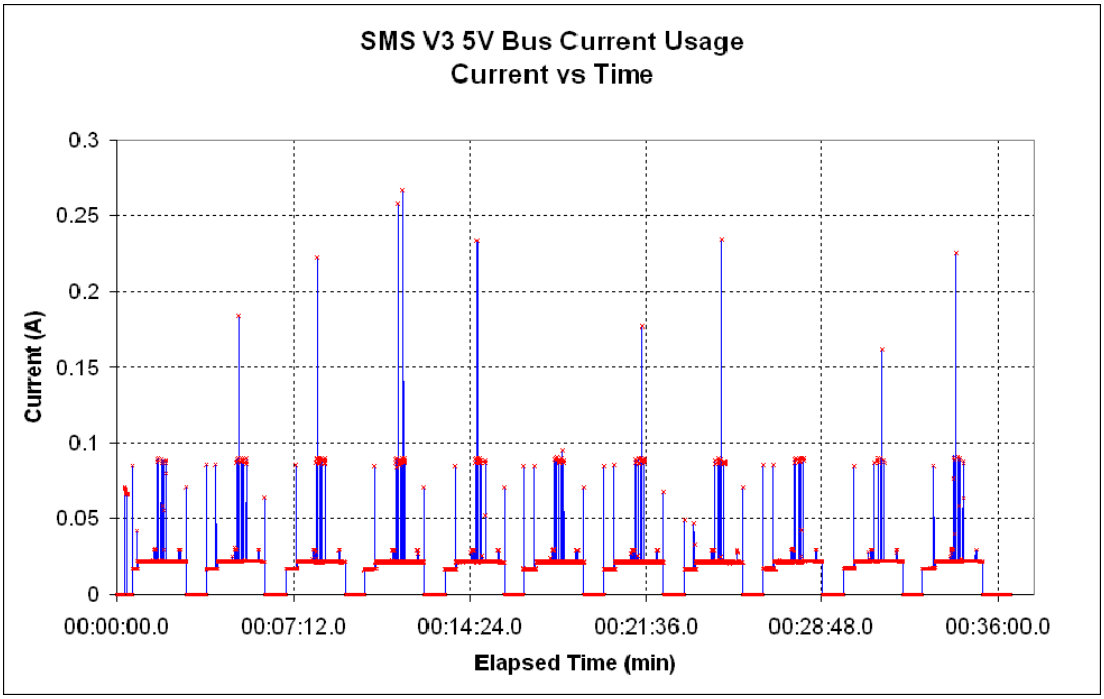

Figure 77 SMS V3 Power Consumption Test Results: 5 V Bus Current

The maximum power draw occurred during the I-V curve algorithm, when the experimental solar cells were switched. This can be seen by the large current spikes in Figure 77. This worst case instantaneous power consumption of the payload was 1.22 W when the current draw was 0.267 A and the bus voltage was 4.56 V. The 3.3 V bus data demonstrated a negligible power use of 9 mW. Another item of note is the fact that the +5 V bus voltage spikes down to approximately 3.5 V at the start of each cycle for a very short period of time. The drop in voltage is most likely caused by the high amount of in-rush current required by the SMS PCB and the +5 V power plane, which powers components such as the sun sensor, voltage regulators, instrumentation amplifiers, and MOSFET relay drivers.

The +5 V bus voltage drop is not seen on the plot in Figure 76 for each cycle because the minimum sampling time of the multimeters was 0.1 seconds, which was not fast enough to catch every single data point during the power consumption test. Also, even though the data from the two plots came from the same experiment, it was gathered using two different multimeters, one for the bus current and one for the bus voltage. The test setup involved connecting each of the multimeters to a PC via a USB

cable. Through this interface, the multimeters were able to be remotely controlled using the Agilent Multimeter Toolbar add-in tool in Microsoft Excel. Because each multimeter required a separate entity of Excel to be running, there was a time drift in the elapsed time between the different data sets. This time drift prevents the two data sets, the current and voltage, from being analyzed together due to a lack of a common reference time.

9. ESP Version Three

The third version of the experimental solar panel refined the previously developed version by optimizing the area available for experimental solar cells. Primarily, the design remained unchanged with only components being rearranged on the actual PCB.

a. Development

After the testing of the ESP V2, ideas were generated to improve the next board and allow for different solar cell shapes to be tested. The development plan for the new circuit board involved keeping the same circuit schematic as used by the ESP V2 to minimize any potential errors. This circuit schematic can be seen in Figure 65. The only difference in the schematic is the naming of experimental solar cell number two; it changed from being a TASC in the version two schematic to being a generic experimental solar cell in version three. Shown in Figure 78 is the revised circuit schematic for ESP V3.

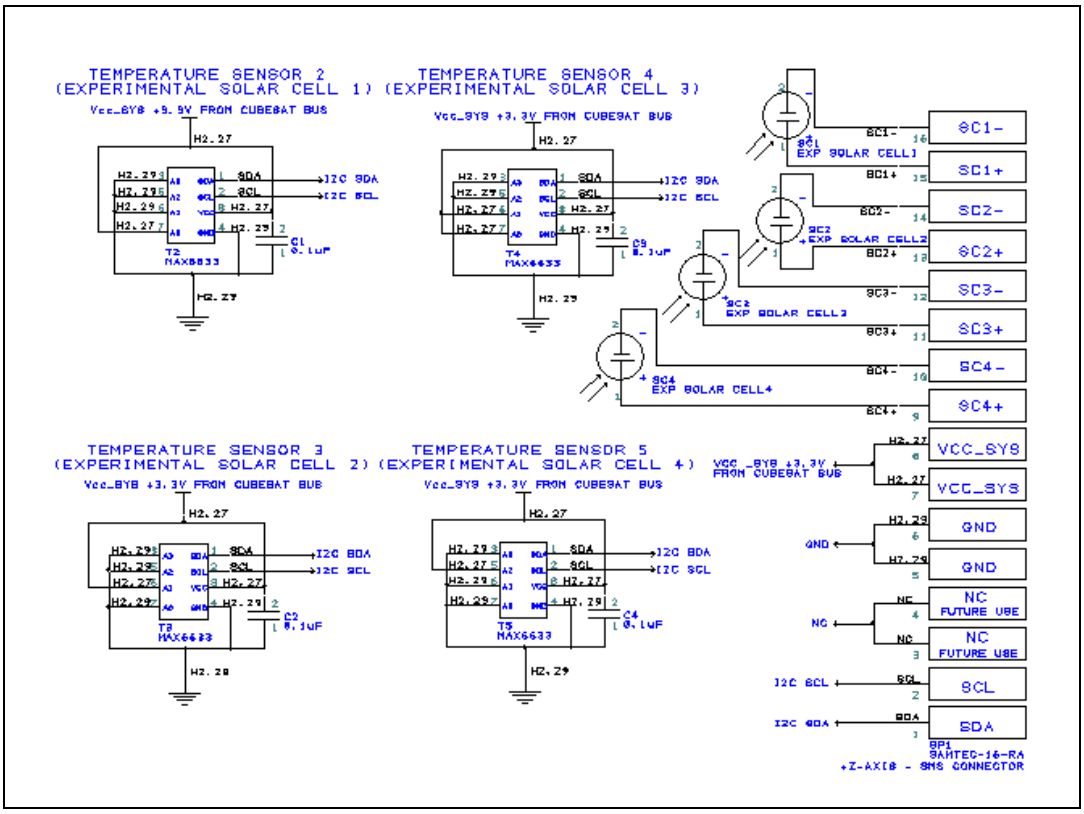

Figure 78 ESP V3 Circuit Schematic

For the PCB layout, the Samtec connector linking the SMS and ESP PCBs was moved to increase the available area for experimental solar cell two. Seen in the picture of the ESP V2 (Figure 66), the reduced area around experimental solar cell two caused by the placement of the connector (the right side of the circuit board) prevents the use of the same shape as the other three cells. The new location of the connector on the ESP V3 allows the usable area for the solar cell to be increased. To ensure all four solar cells have the same area, the shape of the experimental solar cell template (Figure 64) was modified. The revised dimensions, in millimeters, of the new experimental solar cell shape are shown in Figure 79.

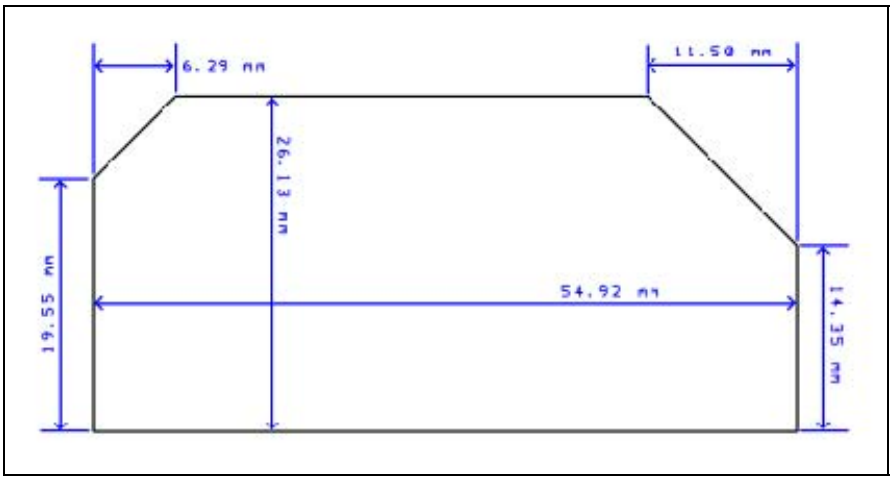

Figure 79 Revised Experimental Solar Cell Dimensions

The circuit board layout contained four temperature sensors, placed in the same location as ESP V2, but the bypass capacitors were moved from the bottom to the top face. Even though these capacitors are tiny surface mount components, the cover plate assembly for ESP V2 needed to be cut to allow the circuit board and structural components to mate properly. With the capacitors on the top, there is no requirement to cut the cover plate assembly in the four locations of the capacitors. The only reason a cut needs to be made in the cover plate assembly is to provide clearance for the sun sensor and the SMS V3 to ESP V3 connector. A silkscreen outline of the single cut was drawn on the bottom of the ESP V3.

b. Design Review

A full design review was conducted for this circuit board, both of the schematic and the PCB layout. The design review was fairly short but brought up several valid points that were incorporated into the final design. The pads of the experimental solar cells were modified to ensure the soldering pads of the chosen experimental solar cells will easily fit without any extra wiring. Also, as a secondary measure, the outlines of a TASC and silicon cell, both used for ESP V2, were placed in all four of the experimental solar cell locations. This allows these solar cells to be used in the event the chosen solar cells are unable to be diced to the proper dimensions. Shown in Figure 80 is the finalized circuit board layout of the ESP V3 PCB.

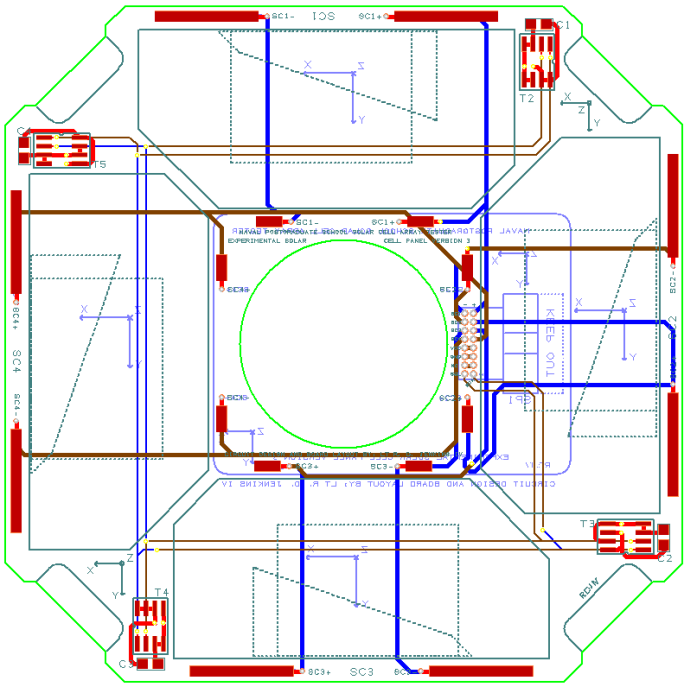

Figure 80 ESP V3 PCB

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IV. SATELLITE INTEGRATION AND TESTING

A. INTEGRATION PROCEDURES

The integration procedures for NPS-SCAT were developed concurrently with the payload development. This was necessary to ensure that the payload would be placed at the proper location within the CubeSat Kit structure and would not interfere with any of the other subsystems. For the most part, the satellite had a straightforward integration plan already outlined by the manufacturer of the CubeSat Kit, Pumpkin Inc. The modular design made the installation of the FM430 and MHX-2400 trivial. However, more planning was required for the placement of the Clyde Space EPS. For nomenclature's sake, the group of PCBs connected together by the CubeSat Bus Connector is referred to as the stack; this is because the subsystem boards stack on top of one another within the CubeSat as seen in Figure 81. The following section is not intended to be used as an integration procedure but rather provides an overview of the steps taken during the integration process; the full NPS-SCAT integration procedure is available in a separate document, the Naval Postgraduate School Solar Cell Array Tester CubeSat Satellite Integration Procedure Version 2.2 [69].

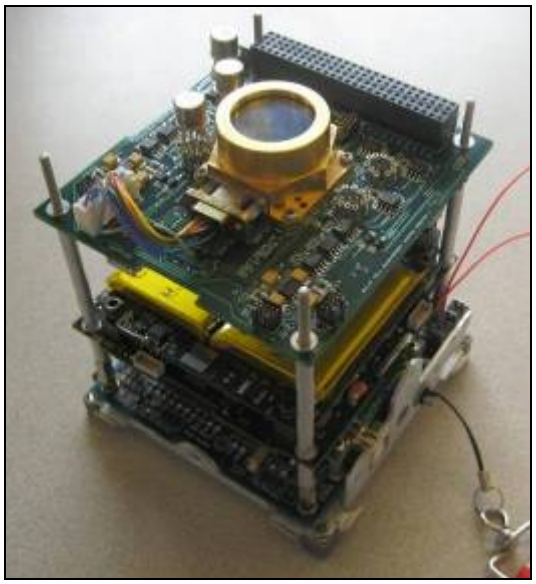

Figure 81 Example of the NPS-SCAT Stack

Prior to assembly of the satellite, the switches on the FM430, the Remove-Before-Flight (RBF) pin, also known as the Pull-Pin, and Separation Switch, needed to be wired to the proper locations to allow for full-functionality, shown for the Pull-Pin in Figure 82. The Pull-Pin was wired in accordance with Table 13 and the Separation Switch was wired in accordance with Table 14. The common pins for both of the switches are all tied together inside the Clyde Space EPS.

Table 13 Pull-Pin Wiring

Pull-Pin Switch Pin	CSK Pin
Normally Closed	H2.33/H2.34
Normally Open	H2.37/H2.38
Common	H2.41/H2.42/H2.43/H2.44

Figure 82 Pull-Pin Wiring

Table 14 Separation Switch Wiring

Separation Switch Pin	CSK Pin
Normally Closed	H2.35/H2.36
Normally Open	H2.39/H2.40
Common	H2.41/H2.42/H2.43/H2.44

The Separation Switch on the engineering design unit (EDU) was not fully wired to the switch inside the CubeSat to allow for ease of handling within the lab and for testing. A wire to the common pin and the normally closed pin on the Separation Switch was soldered to create a simple switch, shown in Figure 83.

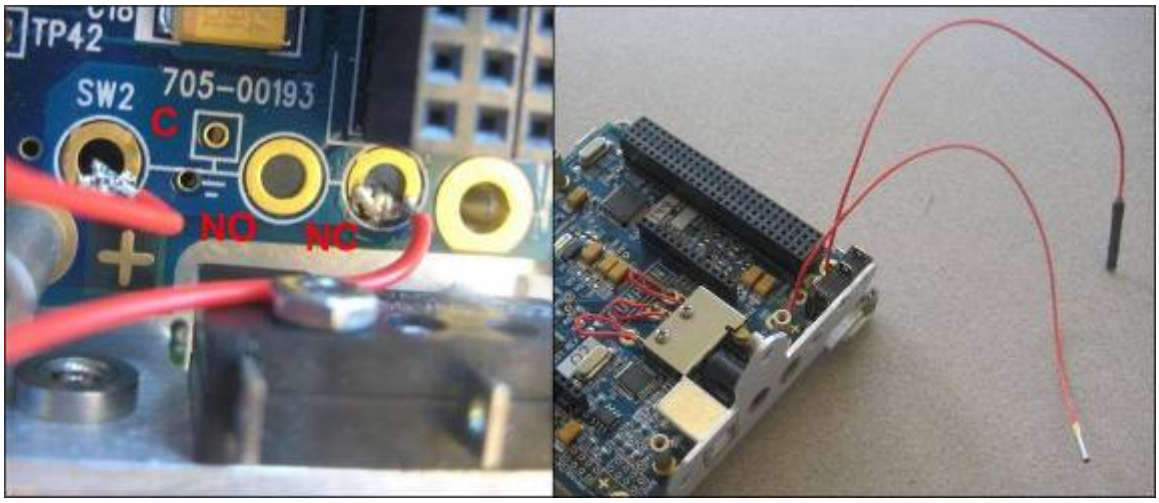

Figure 83 EDU Separation Switch Wiring

The first step in the procedure to assemble the NPS-SCAT satellite is to place the –z-axis solar panel onto the CubeSat Base Plate Assembly. This panel should have any exposed metal (vias, traces, etc) covered with an insulating material such as Kapton tape. It is secured to the structure by four solar panel clips. The –z-axis solar panel was designed specifically to fit in this location, with the placement of the connector in such a location that would prevent any interference with the skeletonized Base Plate Assembly structure.

Once this solar panel has been installed, the FM430 PCB is inserted into the structure and secured using four 15 mm hexagonal stand-offs. The use of these stand-offs is required because they limit the amount of material that can be threaded through the CubeSat structure. Other securing mechanisms, such as the assembly rods, do not have mechanical stops when inserted into the structure and could cause accidental damage to the –z-axis solar panel if allowed to be screwed in to excess.

With the FM430 secured in the Base Plate Assembly, the MHX-2400 transceiver is then placed into the Pumpkin-designed connectors on the FM430 circuit board. Assembly rods were then screwed into the four hexagonal stand-offs to provide circuit board alignment for the entire stack. As the standard assembly rods received in the CubeSat kit were the length of a 1U CubeSat, they were shortened by the length of the 15 mm hexagonal stand-offs.

To prevent the EPS from interfering with the connectors on the remaining solar panels, the EPS circuit board needed to be raised slightly higher than nominally suggested by Pumpkin, Inc. Using two CubeSat Kit Bus Connectors and a 20 mm aluminum spacer placed over each assembly rod, the EPS was positioned at a height that allowed all side solar panels to be installed.

The next circuit board in the stack was selected to be the Beacon PCB. At the time of this writing, the final Beacon PCB has yet to be fully developed. As a placeholder, a Pumpkin protoboard was used instead. This circuit board was placed on top of the EPS using a standard CSK Bus Connector and a standard 15 mm aluminum spacer. To provide full EPS I^2C functionality, two signal lines needed to be shorted on the CSK Bus Connector, shown in Table 15. This was accomplished using the Pumpkin protoboard and will be incorporated into the final Beacon PCB design. Another Pumpkin protoboard with test wiring was inserted into this slot for use in thermal vacuum testing and allowed access to satellite telemetry data.

Table 15 EPS I^2C Net Configuration

Net	Connected To	Use
H1.41	H1.23	EPS SDA
H1.43	H1.21	EPS SCL

To set the SMS PCB, which is placed next in the stack, to a height that allows the sun sensor to be flush with the +z-axis solar panel (the ESP), the pins on the SMS CSK Bus Connector needed to be trimmed by 3.5 mm. Also, to provide support for the SMS PCB, the standard 15 mm aluminum spacers needed to be cut down to a length of 11.5 mm. To provide additional structural integrity for the stack, the Pumpkin, Inc. Midplane

Standoff kit was installed on the top of the SMS PCB. This kit securely attaches the top part of the stack to the CubeSat Kit Chassis Walls. All necessary connectors were then installed onto the SMS, including the three connectors between the EPS and SMS circuit boards. An expanded view of the primary components that make up the NPS-SCAT stack is shown in Figure 84.

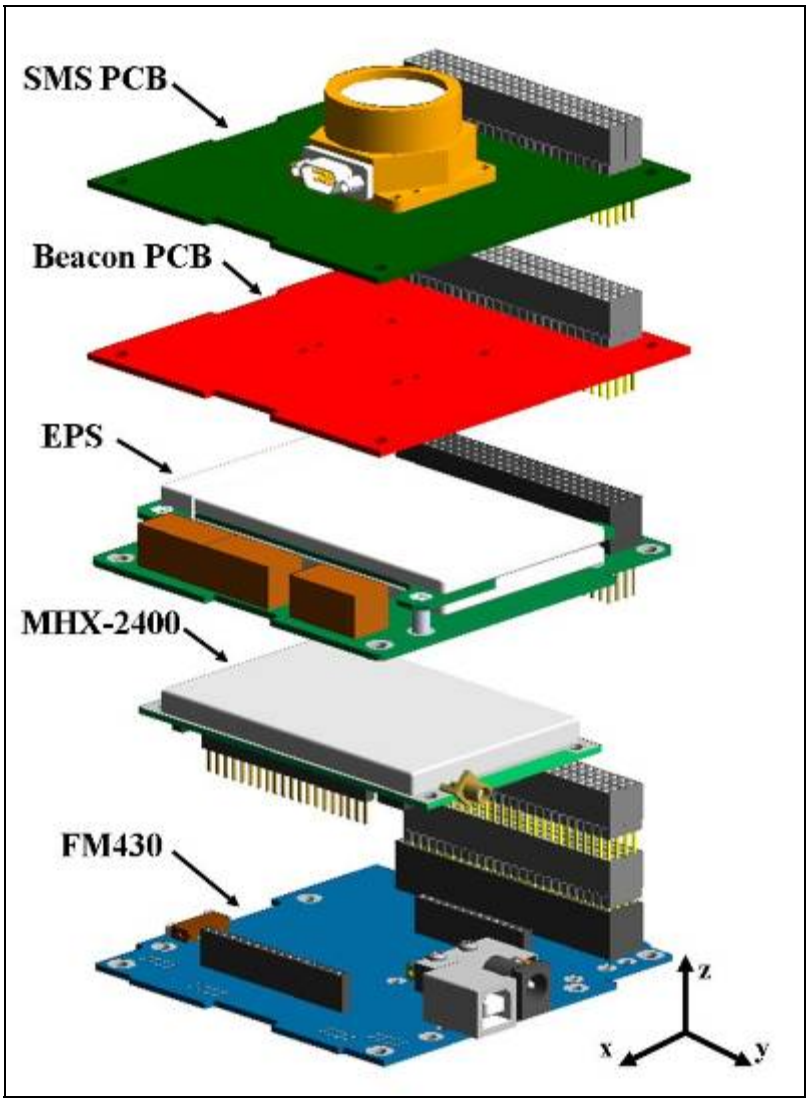

Figure 84 Expanded View of NPS-SCAT Stack

With a fully integrated stack, the Chassis Walls were installed onto the satellite. The side solar panels were then placed in their correct locations on the Chassis Walls and connected to the SMS via Samtec connectors. These solar panels had to be designed to

eliminate any interference between the external components and the CubeSat structure. The solar panel clips on the Base Plate Assembly provided the lower support for the solar panels. With the +z-axis solar panel mated to the Cover Plate Assembly and solar panel clips, this component was then placed onto the stack and provided the upper support for the side solar panels. A CAD drawing of an expanded view of the integrated NPS-SCAT stack with structure and solar panels is shown in Figure 85; the fully integrated NPS-SCAT EDU is shown in Figure 86.

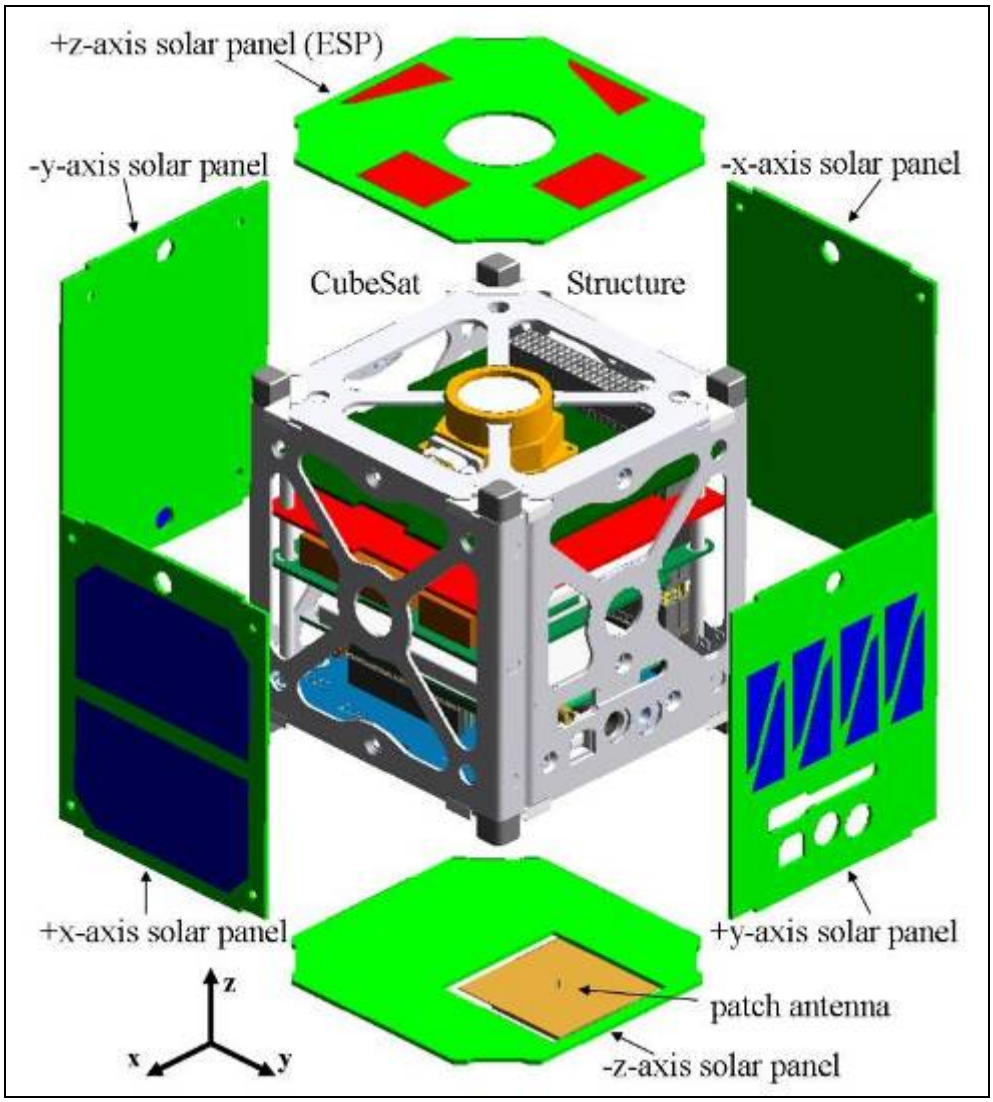

Figure 85 Expanded View of NPS-SCAT EDU

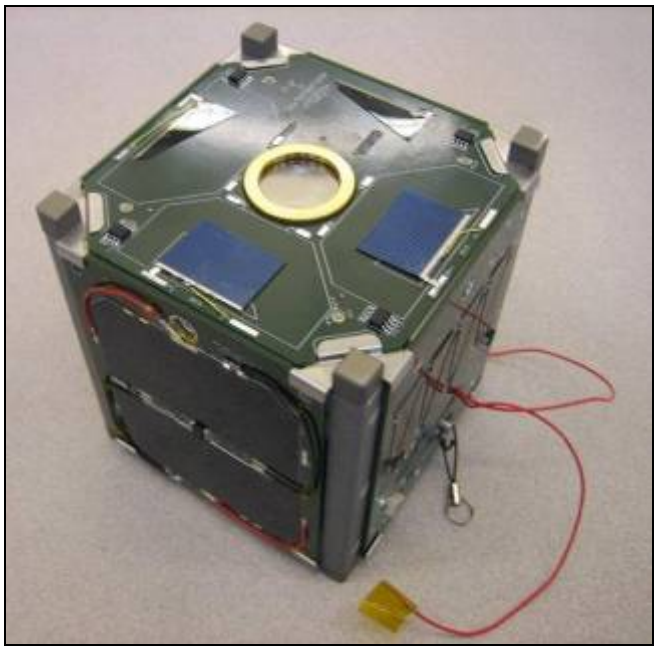

Figure 86 Fully Integrated NPS-SCAT EDU

B. ENVIRONMENTAL TESTING REQUIREMENTS

The initial test plan for the NPS-SCAT EDU was developed based upon rough estimates of the expected launch vehicle requirements. As the satellite has not yet been officially manifested on a flight, the determination of testing requirements rested with the NPS design team. As mentioned in chapter two, the NPS-SCAT CubeSat was offered a possible launch opportunity by the STP onboard the Space Shuttle, which appears to be unavailable. The other, most likely launch opportunity would be onboard a Falcon 1e launch vehicle inside a P-POD-like dispenser. The two possible launch environments differ considerably, depending on if the satellite will be in the SSPL on the Space Shuttle or a P-POD on the Falcon 1e. The worst case environment between these two cases was taken into consideration and testing procedures were developed. The goal of the satellite testing program is to ensure the satellite survives the vibration of the launch environment and the expected thermal environment while in orbit. The intent of the EDU testing was not necessarily to qualify the satellite for flight but to allow the students to become familiar with testing procedures.

1. Vibration Testing

A comparison of the two different launch environments was made using the individual launch vehicle testing reference documents to determine the vibration testing requirements. As the location of the SSPL within the Space Shuttle payload bay was unknown, the entire payload bay was considered in determining the vibration requirements for a Space Shuttle launch. Using Boeing [70], the maximum expected flight level for the Shuttle sidewall was determined. This was compared to the vibration requirements of a P-POD, which are listed in NASA's General Environmental Verification Standards (GEVS) [71]. This document is recommended by Cal Poly as the test levels for the P-POD launch environment on an EELV, as stated by Marissa Brummitt [72]. It was found that the testing requirements listed in GEVS were more restrictive than those in Boeing, and were chosen as the vibration testing guideline for the NPS-SCAT satellite [72].

2. Thermal Vacuum Testing

A similar comparison was conducted for the thermal environment testing requirements [72]. The thermal environment experienced by the NPS-SCAT CubeSat while in the SSPL in the Space Shuttle payload bay will be quite different from that of the Falcon 1e. This is due to the fact that in accordance with the flight plan of the Space Shuttle, small satellites are not deployed until after the orbiter has undocked from the International Space Station (ISS), which occurs late in the flight timeline. This will result in the satellite experiencing a possible extreme thermal environment for approximately two weeks, depending on the placement of the Space Shuttle while docked with the ISS. A review of the data from the nanosatellite produced by the Aerospace Corporation, the Pico-Satellite Solar Cell Testbed, which launched from the Space Shuttle using the SSPL, produced numbers of the expected thermal environment, between -23°C and 35°C [73]. For a P-POD launch, the requirements outlined by Cal Poly only specify the satellite undergo testing in accordance with NASA GEVS as well as experience a thermal bake-out prior to spacecraft delivery [71, 72].

Based upon Space Shuttle worst case temperatures and the test levels and durations described in the MIL-STD-1540E, the thermal vacuum testing requirements for the NPS-SCAT EDU were determined [74]. Using a Tenney Space Jr. manually controlled, thermal vacuum chamber, several thermal vacuum (TVAC) tests were conducted on the satellite.

C. TESTING PROCEDURES AND RESULTS

The thermal vacuum and comprehensive performance tests conducted on the NPS-SCAT EDU were created as a team effort by Brummitt, Jordan, and the author. As previously mentioned, the requirements for the TVAC testing were developed using the applicable NASA and Cal Poly reference documents. The final test plan used a version of the requirements, modified to meet the thermal envelope of the components within the satellite, keeping the temperatures within the component storage and operating temperatures. With these modified test limits, the TVAC tests conducted on the NPS-SCAT satellite would not necessarily meet the NASA standards required for launch onboard a human-qualified LV but would provide data that can be used for future testing. Two tests were conducted on NPS-SCAT using the Tenney Space Jr. thermal vacuum chamber; a workmanship test during which the satellite was off, and an operational test during which the satellite was fully functional and in an operational state. Both tests had similar profiles, which entailed a pressure of less than 10-5 torr, a thermal hot soak at 60°C for one hour, a functional test at ambient temperature, a cold soak at -20°C for one hour, and a final functional test at ambient temperature and pressure [75].

1. Test Setup Development

To access the housekeeping data of the satellite while it was in the TVAC chamber, a harness was needed to access the several different pins on the CSK Bus Connector. A Pumpkin, Inc. protoboard, placed in the Beacon PCB location within the CubeSat stack, was used to link the harness wires to the CSK Bus Connector. The harness was made to connect to a special connector passing wires through the TVAC chamber walls without compromising the chamber's operation [76]. The list of data chosen to be accessed is listed in 0. Several multimeters were used to monitor the

parameters of the satellite, including the +5 V and +3.3 V busses, the battery voltage, and the battery current. The three solar array connectors were attached to power sources in accordance with the Clyde Space EPS manual, which allowed the battery to be charged while the satellite was in the chamber, simulating solar panel power production [54]. The two Beacon I^2C lines (SDA and SCL) were incorporated into the harness for future use, as the Beacon PCB was unavailable at the time of TVAC testing. The fully integrated NPS-SCAT EDU with the TVAC test harness is shown in Figure 87.

Table 16 TVAC Test Harness Pin Descriptions (From [76])

Pin	Use
H2.11	Beacon SDA
H2.12	Beacon SCL
H2.25	+5 V Bus
H2.27	+3.3 V Bus
H2.29	Ground
H2.32	-Battery
H2.33	+Battery
H2.35	-Separation Switch
H2.41	+Separation Switch
SA1	Solar Array 1
SA2	Solar Array 2
SA3	Solar Array 3

Figure 87 TVAC Test Harness Installed in NPS-SCAT

In addition to the harness, a stand-off was required to thermally isolate the satellite from the chamber supports. Delrin plastic, a thermally non-conductive material with a very high melting point, was chosen to be used for the stand-off. The stand-off was created with four indentions to allow the CubeSat feet to be inserted, ensuring the satellite was secure throughout the test [77]. The test setup already installed in the TVAC chamber included an aluminum cold plate, used to decrease the time it took to lower the chamber temperature, and several thermal heater strips, used to help increase the temperature of the chamber more quickly. This setup was not modified and was used for the workmanship test. The final configuration prior to the workmanship TVAC test is shown in Figure 88.

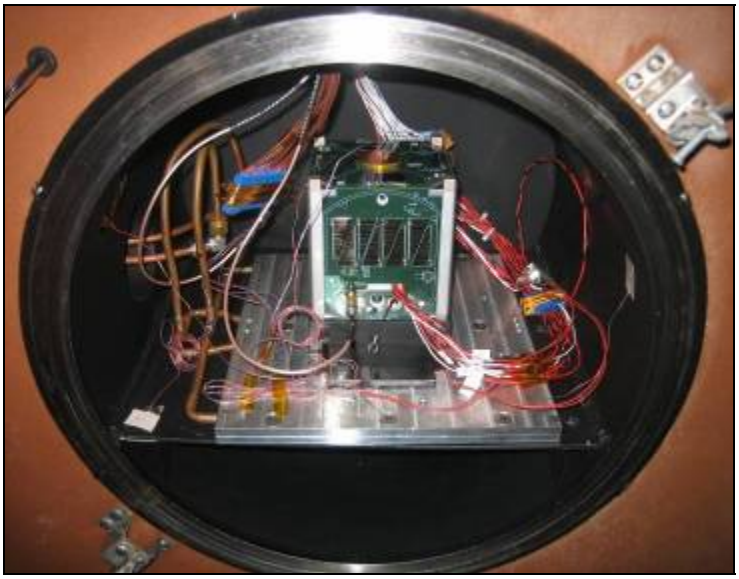

Figure 88 Workmanship TVAC Test Configuration

2. Workmanship TVAC Test

The workmanship TVAC test was conducted on the NPS-SCAT EDU using the above test setup. With the procedures for the Tenney Space Jr. TVAC chamber, the planned profile was executed, using four thermocouples placed inside the chamber to monitor the temperature. The chamber was first evacuated to a pressure of 10-5 torr. As can be seen in Figure 89, the four thermocouples tracked together and allowed the test monitors to accurately conduct the test. Once one of the thermocouples reached 60°C,

this temperature was held for an hour before being brought back to ambient temperature (about 23°C). A functional test of the satellite was then successfully conducted by powering the satellite on using the Separation Switch through the test harness. The chamber was then lowered to a temperature of -20°C, which was held for an hour. After the cold soak, the temperature and pressure were brought back to ambient values. The final functional test verified the satellite was still fully operational.

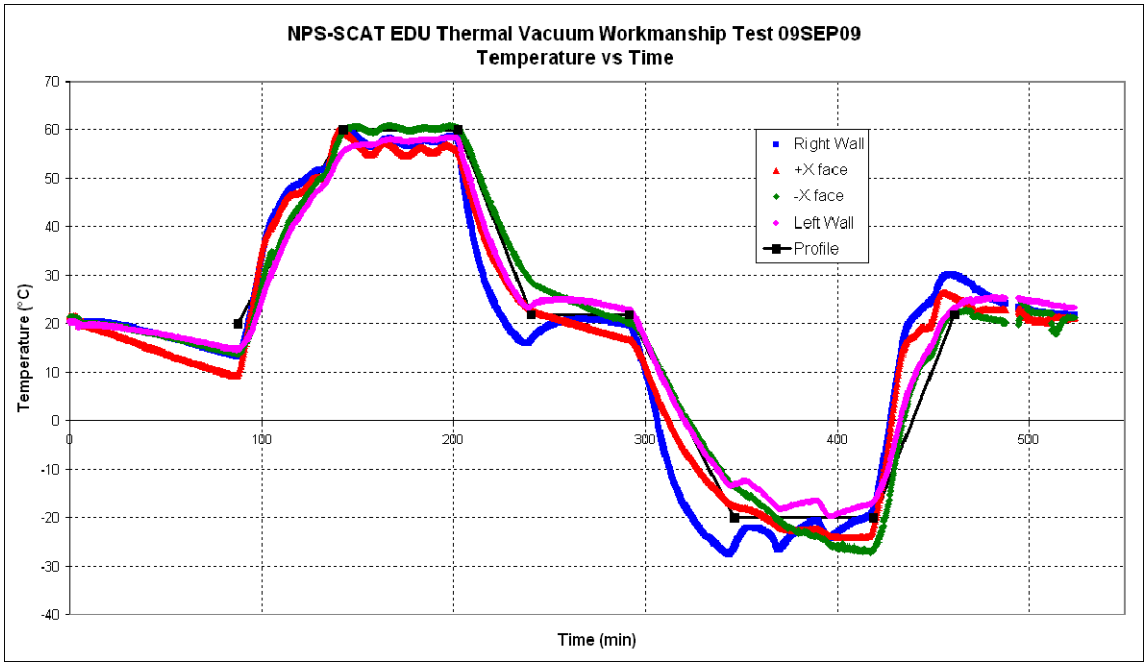

Figure 89 Workmanship TVAC Test Results

Upon visual inspection of the NPS-SCAT EDU, it was found that the heater strips on the aluminum cold plate, located directly underneath the Delrin stand-off during the test, had heated up to a temperature above the melting point of Delrin (approximately 175°C) and melted a portion of the stand-off, shown in Figure 90. In addition to damaging the stand-off, the melted Delrin had off-gassed into the chamber and the heater strips had become unusable. It was determined that the heater strips were not secured properly secured to the cold plate, preventing the heat being produced by the strips from being absorbed by the aluminum and instead caused it to be absorbed by the Delrin, which melted.

Figure 90 Melted Delrin Stand-off

3. Operational TVAC Test

After the workmanship test, several modifications were made to the TVAC test configuration. To ensure the chamber was cleaned of material that might have off-gassed during the workmanship test, a bake-out was conducted at 60°C for approximately one hour. Prior to re-insertion into the chamber, the NPS-SCAT EDU was disassembled and cleaned. Figure 91 shows the deposits of Delrin on the –z-axis solar panel which resulted from the Delrin melting while the satellite was in the TVAC chamber.

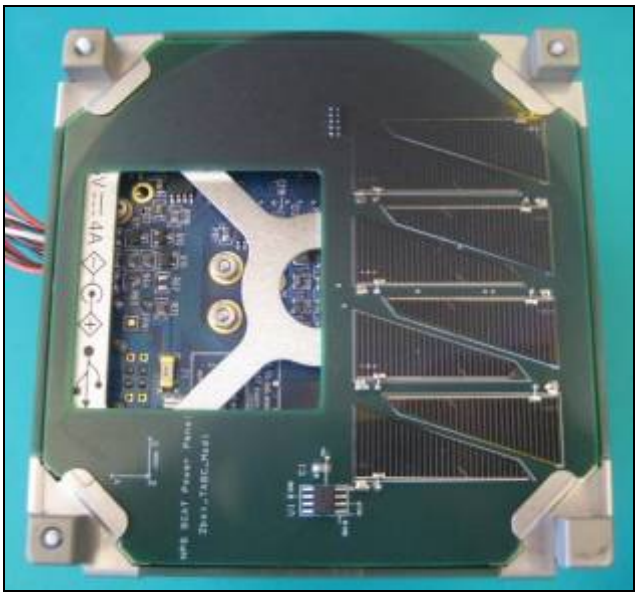

Figure 91 Post-Workmanship TVAC Test (-z-axis solar panel)

A modified chamber setup was developed, with the aluminum cold plate and heater strips removed from the chamber leaving just the CubeSat and Delrin stand-off. Four lifting bolts were used to elevate the stand-off to a height which, when placed into the TVAC chamber, would place the NPS-SCAT satellite in the center of the chamber. The modified stand-off is shown in Figure 92 and the operational TVAC test configuration with both the stand-off and satellite in the chamber is shown in Figure 93.

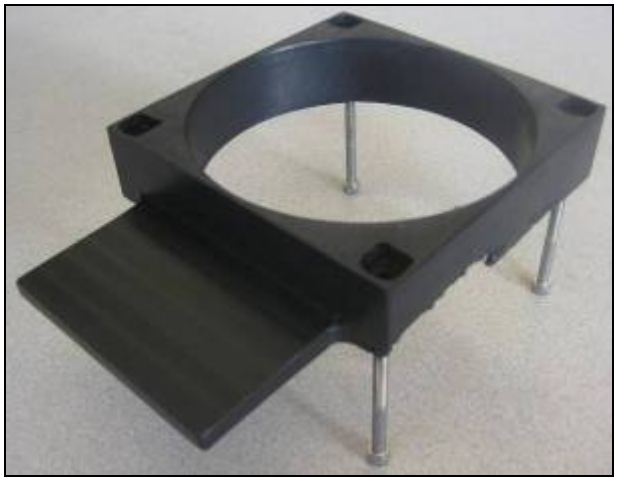

Figure 92 Modified Delrin Stand-off

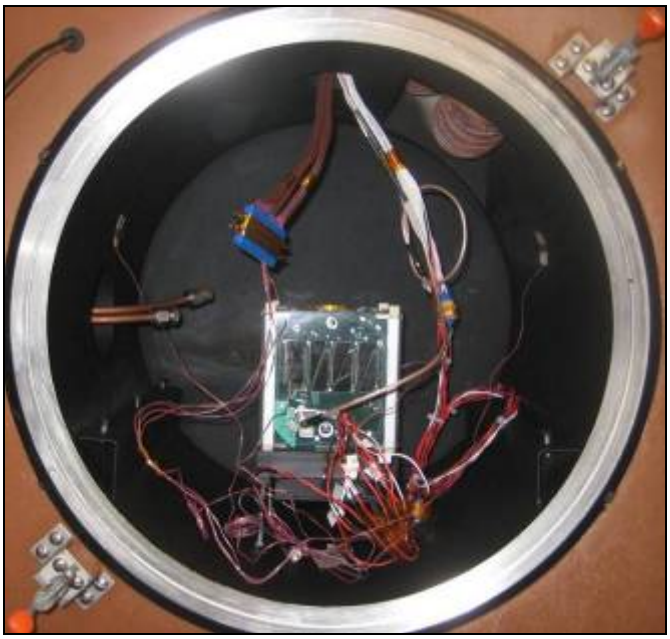

Figure 93 Operational TVAC Test Configuration

The operational TVAC test consisted of the same profile used for the workmanship TVAC test but with the satellite on and functional for the entire cycle. Because the satellite was on, the operational component temperature limits were more restrictive than the storage limits, which were used for the workmanship test. The components that imposed these limits were the two batteries; the EPS lithium polymer battery and the SMS RTC coin cell. The EPS battery must not be hotter than 55°C or cooler than 0°C; the SMS RTC coin cell must not go below -20°C. This test also verifies the functionality of the built-in battery heater on the EPS that is designed to keep the battery above its lower temperature limit of 0°C. In addition to the four thermocouples used to monitor the chamber temperature, the sixteen temperature sensors located on the satellite were used to gain a complete picture of satellite temperature. A plot of the active temperatures overlaid with the profile is shown in Figure 94. The satellite functioned throughout the test. During the cold soak, the power sources simulating solar array power needed to be turned on to charge the battery. The battery voltage, which was being continuously monitored, had dropped below 7.4 V and the cold temperature increased the battery discharge rate, necessitating an external power source to continue

the test. It can be seen in the plot that the battery heater did energize when the battery temperature, shown in yellow, dropped to approximately 3°C and turned off once the temperature had increased to about 5°C.

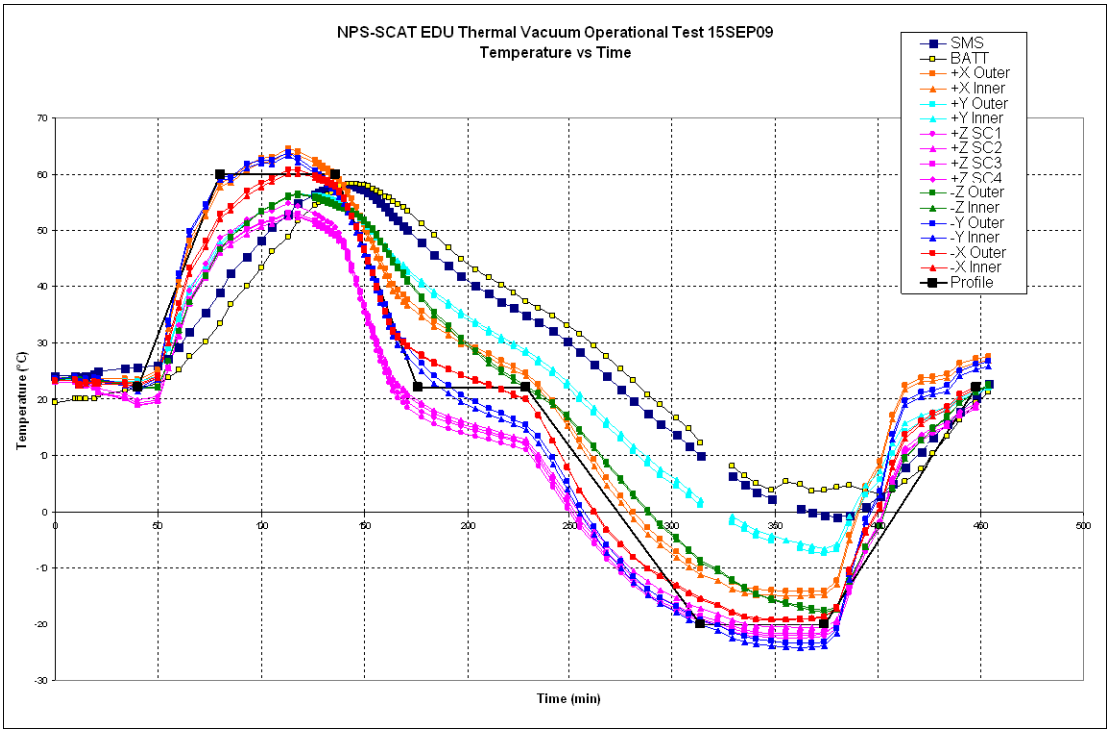

Figure 94 Operational TVAC Test Results

4. Comprehensive Performance Test

To test the basic functionality of the software and its control of the hardware, a comprehensive performance test (CPT) was executed. Software was developed by Nathan Moshman to follow a simplified concept of operations for the NPS-SCAT satellite to produce as close to a fully functional satellite as was possible with the available hardware [78]. The goal of the test was to verify that the satellite could continuously take I-V curves, temperatures, sun angle data, read EPS telemetry, communicate this data to the ground station, and maintain this functionality for as long as the test was run, i.e. maintain the battery charge at a functional level. Starting out with the fully integrated NPS-SCAT EDU, the three side solar panels with large area CIC solar cells were removed from the Chassis Walls and placed together to face the sun. These panels remained connected to the satellite to provide power to charge the battery.

The remaining part of the satellite was placed at an angle, pointing the +z-axis towards the sun at the start of the test. The satellite was then turned on to begin data acquisition and left for approximately five hours, as shown in Figure 95.

Figure 95 Comprehensive Performance Test Configuration

The resulting data produced by the satellite's five hour run in the sun was post-processed using MATLAB by Moshman and is displayed in Figure 96. Each of the subplots represents one of the four experimental solar cells. Solar cells one and two are TASC and three and four are made of silicon. The three-dimensional plot combines the I-V curve, temperature, and sun angle data of the experimental solar cells. The axes labeled "Solar Cell Current" and "Solar Cell Voltage" represent the typical I-V curve axes of solar cell current and voltage, respectively. The type of solar cell can be determined by looking at the x-axis; TASC produce a maximum voltage of approximately 2.5 V while silicon cells produce about 0.5 V. The group of I-V curve data was paired with the sun angle, represented by the y-axis in the plot, which is labeled as "Sun Vector Z Component." With this information, the I-V curves were then plotted as a surface in 3D space. The temperature of the solar cell was also grouped in with the I-V curve and sun angle pair, represented by the color of the I-V curve/sun angle surface. Time can also be inferred by the sun angle component, which is the cosine of the sun angle. Notice that it begins around 0.9, moves towards 1.0 (the maximum value

corresponding to a sun angle of zero degrees), and then decreases back to a number slightly more than 0.95; this represents the changing sun angle due to the earth's diurnal rotation.

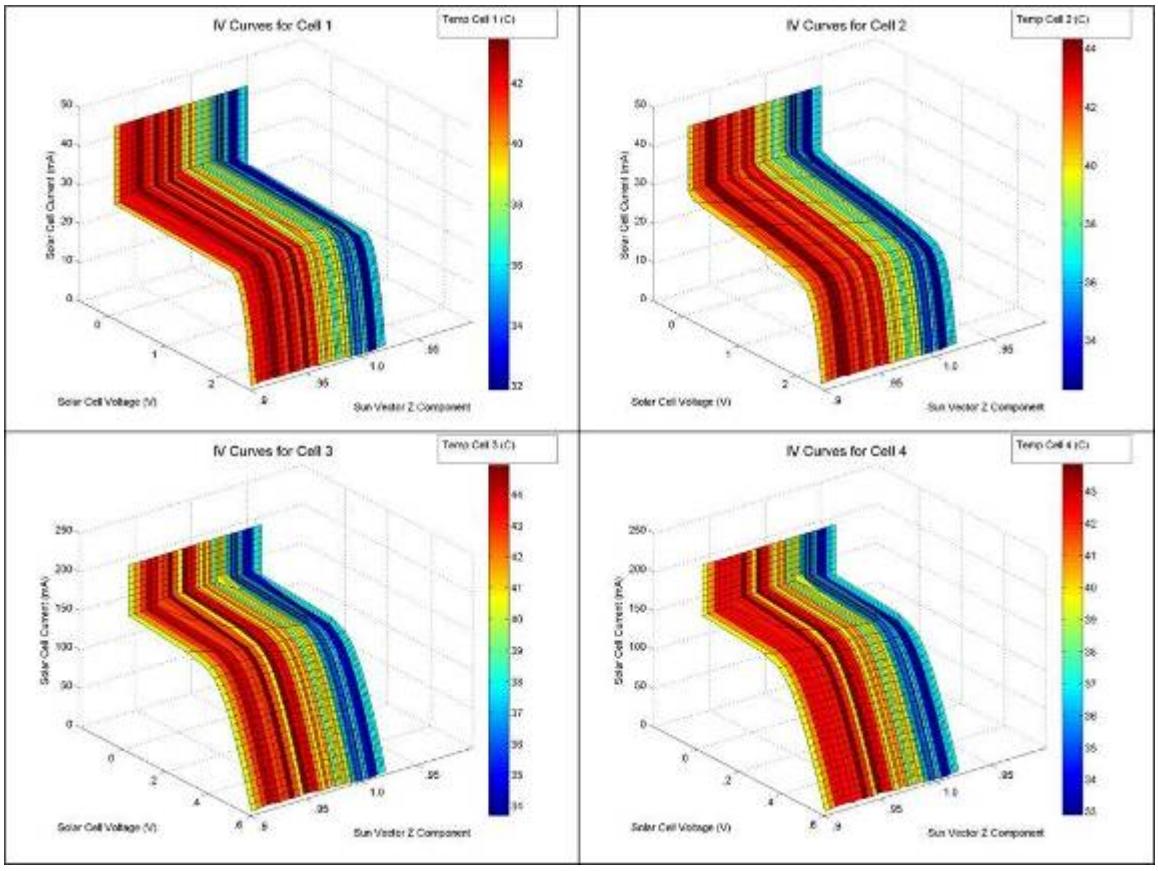

Figure 96 Comprehensive Performance Test Results (After [79])

A plot of only the sun angle versus time is shown in Figure 97. The odd points on either end of the smooth curve occurred during the CPT set-up and conclusion, and are not displayed in the 3D I-V curve plots. Clearly, NPS-SCAT's sun sensor was able to track the apparent motion of the sun as seen by the smooth curve portion of the plot.

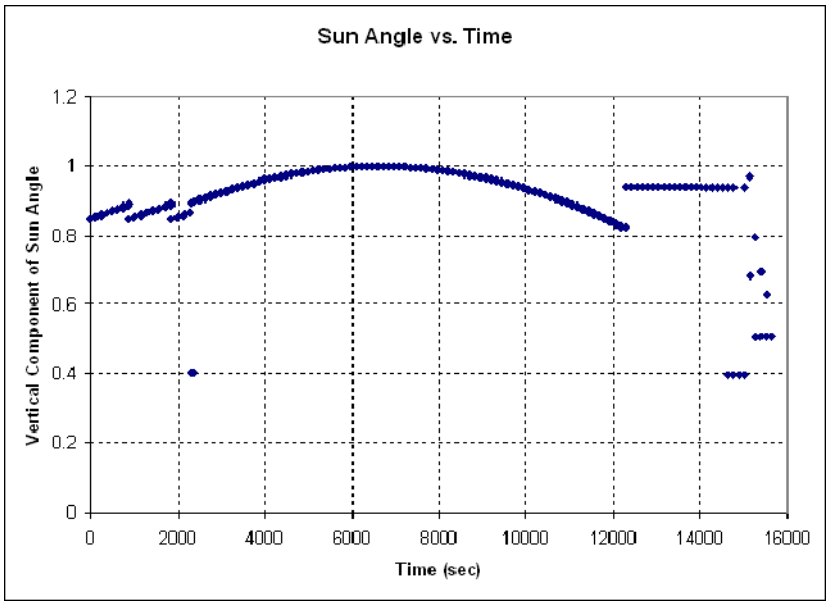

Figure 97 Sun Angles from Comprehensive Performance Test (From [79])

The results can now be analyzed to determine how the experimental solar cells performed during the entire CPT. Early on in the test, represented by the I-V curves closest to the origin of Figure 96 (the left-most side of the axis labeled "Sun Vector Z Component"), the experimental solar cells heated up quickly. This was due to the fact that it was near local apparent noon (approximately 10:30 am) and the sun's rays were passing through less atmosphere. As the sun angle measured by the sun sensor neared zero degrees (1.0 on the axis labeled "Sun Vector Z Component"), the temperature of the solar cells began to drop. This was caused by two factors: a) it was late afternoon and the wind began to pick up, causing convective cooling of the solar cells, something that would not be experienced in space and, b) the actual sun angle was low in the sky, resulting in the sun's rays having to pass through more atmosphere and reducing the overall radiance. The drop in radiance is also demonstrated by the drop in solar cell current.

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V. CONCLUSIONS AND FUTURE WORK

A. SUMMARY

This thesis chronicles the development of the Naval Postgraduate School Solar Cell Array Tester CubeSat from prototype stage to a nearly complete engineering design unit with particular emphasis on the solar cell measurement system payload and the thermal analysis. The payload required development of both the solar cell measurement system printed circuit board and the experimental solar panel printed circuit board, and ended up driving the integration of the other subsystems, especially the solar panels and electrical power subsystem.

Each subsystem was tested to verify functionality prior to integration. To integrate the commercial-off-the-shelf and custom subsystems, steps were taken to ensure proper fit in the CubeSat Kit. Finally, comprehensive performance tests were completed on the integrated engineering design unit, verifying that the satellite's systems could work together.

To gain a better understanding of the thermal environment the satellite is expected to encounter, a simplified thermal model of NPS-SCAT was developed. Using the information from the thermal model, data from on-orbit satellites, and launch vehicle requirements, a thermal vacuum test plan for the engineering design unit was developed and executed using the facilities within the NPS Small Satellite Laboratory. In addition to the technical work accomplished by the author, the educational model of student teams working together in different roles was validated, having provided a great deal of hands-on education for all involved.

B. PAYLOAD DEVELOPMENT AND REFINEMENT

Even though the design for the payload has been set for the first NPS-SCAT flight unit, several modifications could be made to allow more functionality for a future flight unit design. Currently, the experimental solar panel is not able to produce enough voltage to be useful in powering the satellite when not running I-V curves. The battery charge regulators on the EPS require a minimum of 3.5 V and the ESP only produces

about 2.5 V from the Spectrolab Triangular Advanced Solar Cells. To allow the ESP to charge the battery when not undergoing a test, additional TASC solar cells could also be placed on the panel. There are two unused pins on the ESP-to-SMS connector (labeled NC in Table 11), which could be used to feed the output of these solar cells to the SMS-to-EPS connector, providing a path for the solar cell power to charge the battery.

The relays on the SMS PCB used to switch the experimental solar cells between the EPS and the SMS circuitry could better reconfigured. Instead of using one relay for one solar cell, the dual-pole design of the relays could switch two experimental solar cells with one relay by tying the solar cell negative leads together. This would remove two relays and two MOSFET relay drivers, opening up area on the PCB for an easier layout or other components.

Additional research could be conducted on the components selected to create the SMS circuit to locate parts that have an even lower power consumption rating. Even though the components currently in use are rated for low power, there are several components that were not explicitly optimized for the circuit, such as the AO4440 MOSFET, the buffer drivers, and the real-time clock (RTC) circuitry. The choice of the power source for the RTC, a 3.0 V coin cell, was also not optimized for space flight. This coin cell is a separate power source from the EPS battery and, upon installation, will provide uninterrupted power to the RTC for approximately two years. However, as this particular Li-ion cell has not flown in space before, and Li-ion cells have the potential to be problematic with issues of thermal runaway if improperly configured, there may be issues with the safety certification [80]. The RTC could be powered using the onboard CubeSat 3.3 V bus on the SMS V3 by fitting R100 with a 0 Ω resistor. However, if powered this way, the RTC will need to be reset every time the satellite power is cycled. This is not ideal; better might be to use the EPS battery directly to power the extremely low power RTC or to use a spaceflight-qualified Li-ion coin cell.

C. SUBSYSTEM TESTING

Several subsystem components of the NPS-SCAT EDU still require more testing to understand their functionality and behavior in the expected environments.

1. Payload

As mentioned previously, the ESP V3 has been designed, has undergone a design review, and the manufactured circuit board has been received. It now needs to be populated with temperature sensors and the final experimental solar cells. It will then need to be tested. The final experimental solar cells should be fully tested using the SMS circuitry under a solar simulator and the results fully documented, thereby understanding the cells' baseline performance and enabling accurate comparisons throughout their on-orbit testing.

The SMS V3 EDU PCB should undergo a vibration test to analyze how the circuit board structure responds in a simulated launch environment. The primary concern is whether the current height of the relays will cause problems. Because the relays are several millimeters above the circuit board, this height differential may cause the relay leads to fail during the vibration test. A mass model of the sun sensor should be used during the qualification level vibration test to prevent possible damage to the EDU sun sensor.

In preparation for the flight unit testing, the flight version of the SMS V3 PCB must be constructed and tested. The resistors for the SMS circuits need to be customized for each type of experimental solar cell. This sets the maximum amount of solar cell current that can be measured by the SMS circuit. Prior to soldering the components to the SMS PCB, all items should be placed in a bake-out chamber and heated. This will allow the components to off-gas prior to assembly.

As mentioned in the SMS V3 testing section, the power consumption test produced data that indicates the +5 V bus spikes down to a dangerously low level of 3.5 V when the SMS PCB is powered on. This data, along with the problems mentioned in chapter three, suggest this test should be redone using a test setup that would eliminate any time drift and allow the data to be fully analyzed. However, using the data that is currently available, the problems that might occur to the satellite due to this issue are worth mentioning. Because the communications subsystem is known to use the most power, if the SMS V3 were to be powered on during a communications pass, the drop in

voltage might be low enough to cause a restart of the MHX-2400 or even the entire satellite. To prevent this from happening, the software should ensure no other subsystem is running, including the MHX-2400 and Cal Poly Beacon, whenever the SMS V3 is energized. Conversely, if the satellite is in a communications window, the SMS V3 should not be powered on until the satellite has ceased transmitting and the battery voltage is at an appropriate level.

2. EPS

The Clyde Space 1U EPS1 has been found to have several issues through in-house testing. Further testing to determine the battery capacity of the two lithium polymer cells as well as charge and discharge cycling is necessary to obtain a complete understanding of the system. Also, when the Pull-Pin is removed to create the flight configuration, the parasitic load of the BCRs will be constantly active. A newer version of the 1U EPS has been developed by Clyde Space fixing this problem and providing additional functions such as enabling different configurations for the Pull-Pin and Separation Switch. Testing of this device should occur before being integrated into the satellite.

3. Communications

Once the Beacon PCB has been received, it will need to be fully tested using the Amateur band ground station. The hardware that will enable the beacon antenna to be deployed and transmit data needs to be fully identified and installed on the +y-axis solar panel. The software and hardware will then have to be integrated and tested for full functionality. The integration of these components into the CubeSat stack will need to be completed and any issues identified as soon as possible so that they can be corrected.

The MHX-2400 patch antenna and Beacon half-wave dipole antenna radiation patterns need to be determined. This can be done using the NPS anechoic chamber located in Spanagel Hall [40].

D. TESTING FOR LAUNCH VEHICLE

1. Vibration

The NPS-SCAT EDU and flight unit should be fully tested using the NPS shaker to simulate the launch environment in accordance with the testing requirements called for by the launch vehicle. The EDU should serve as the model on which to verify the procedures.

2. TVAC

A final TVAC test of the EDU and flight unit to launch vehicle specifications needs to be conducted. Based upon the flight opportunity and specific launch requirements, the different levels for each test can be determined.

3. EMI

The requirements for electromagnetic interference (EMI) testing are defined by the launch vehicle. The NPS-SCAT CubeSat should not require testing in this area as all systems are powered off for launch and the satellite will not power up its communication subsystem for at least 30 minutes following deployment [1], [40].

4. Thermal

As part of this thesis, the single node thermal model of the NPS-SCAT CubeSat was created providing some insight into the expected thermal characteristics of the satellite. A more detailed model was created by NPS students in AE3804 during the winter quarter of Academic Year 2010, incorporating 20 nodes. This model resulted in a similar on-orbit thermal profile to the single node model but still made some assumptions based upon the expected satellite tumble rate. To better predict the satellite's on-orbit thermal characteristics, the simulation capabilities of I-DEAS should be used on an accurate CAD model of the satellite.

E. ANALYSIS OF THE CUBESAT PROJECT

At the project's inception, the choice to use primarily COTS components in the construction of the satellite allowed the students to focus more on the integration of the

subsystems and payload. By keeping the satellite to the relatively small size and complexity of a CubeSat, the entire lifecycle of the satellite could possibly be experienced by a single student. For the first CubeSat built at NPS, however, the timeline has been extended due to the nature of a first generation program: working through the issues of developing and testing real hardware. The hands-on education provided by the NPS-SCAT satellite, including mission planning, hardware construction, and testing, helped reinforce the knowledge developed during the preceding coursework and provided additional skill development opportunities to the students involved.

Through the knowledge gained in the design and construction of the NPS-SCAT satellite, NPS will be able to more easily create a standardized CubeSat bus that can be integrated with more advanced payloads. When placed in the relatively low cost CubeSat form factor, these payloads could serve as risk mitigation and technology readiness level advancement opportunities for a multitude of research areas including attitude control or adaptive optics.

In addition to the practical portion of the project, the structure of the satellite design team added a real-life dimension to the project. With a program manager to keep track of the budget and schedule and support engineers to work the different subsystems, the team approach helped to model how an actual program of record for the Department of Defense would function. As the team is small enough that everyone can follow the progress of the other students, this approach produces well-rounded students who could easily move on to become a productive member of the DoD Space Cadre.

APPENDIX A: CIRCUIT BOARD COMPONENT LISTS

SMS Circuit Component List (Version 1)

Part Number	Name	Package	Purchase Required?	Quantity
1 M Ohm	Resistor	Surface Mount (1206)	N	2
49.9 Ohm	Resistor	Surface Mount (1206)	N	2
10 uF	Capacitor	Surface Mount (6032)	N	8
0.01 uF	Capacitor	Surface Mount (0805)	N	4
0.1 uF	Capacitor	Surface Mount (0805)	N	4
OP97EP	OpAmp	DIP	N	2
AD620AN	Instrument Amp	DIP	N	2
MAX680CPA	Voltage Converter	DIP	N	2
WM18928-ND	MOLEX 8-pin Male Connector	Through Hole	N	3
STPS0520Z	Schottky Rectifier	Surface Mount (SOD-123)	N	4
2N6796	MOSFET	Through Hole	N	2
			TOTAL	35
Connectors:				
WM5989-ND	MOLEX 8-pin Female Connector	Through Hole	N	3

SMS Circuit Component List (Version 2)

Part Number/Type	Name	Package	Purchase Required?	Quantity	O/H
1 M Ohm	Resistor	Surface Mount 1206	N	2	Y
10k Ohm	Resistor	Surface Mount 1206	N	2	Y
20k Ohm	Resistor	Surface Mount 1206	N	10	Y
100k Ohm	Resistor	Surface Mount 1206	N	2	Y
SMS Ckt 1 X Ohm	Resistor	Surface Mount 1206	N	1	Y
SMS Ckt 2 X Ohm	Resistor	Surface Mount 1206	N	1	Y
10 uF	Capacitor	Surface Mount 3528	N	8	Y
0.01 uF	Capacitor	Surface Mount 0805	N	9	Y
0.1 uF	Capacitor	Surface Mount 0805	N	10	Y
STPS0520Z	Schottky Rectifier	SOD-123	N	6	Y
OP97FSZ	OpAmp	SOIC	N	2	Y
AD620ARZ	Instrument Amp	SOIC	N	2	Y
MAX6633MSA	Temperature Sensor	SOIC	N	1	Y
MAX680ESA+	Voltage Converter	SOIC	N	2	Y
AO4440	MOSFET	SOIC	N	2	Y
MAX4427ESA+	MOSFET Driver	SOIC	N	5	Y
ER422D	Latching Relay	Through Hole	Y	5	Y
WM18926-ND	MOLEX Connector (male)	Through Hole	N	1	Y
FTSH-105-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	5	Y
FTSH-108-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	1	Y
DF13-6P-1.25DSA	Hirose Connector (male)	Through Hole	N	3	Y
VL2320-1F2N	Coin Cell	Surface Mount	N	1	Y
ABS10-32.768KHZ-1-T	Crystal	Surface Mount	N	1	Y
PCA8565TS	Real Time Clock	TSSOP	N	1	Y
SNLVC245APWR	Octal Bus Transceiver	TSSOP	N	1	Y
SN74LVC2G04DBVR	Dual Inverter Gate	SOT-23	N	1	Y
PCA9517DR	I^2C Bus Repeater	SOIC	N	1	Y
SN74LVC126APW	Quadruple Bus Buffer Gate	TSSOP	N	1	Y
			TOTAL	87	
Connectors:					
FFSD-05-D-X.00-01-N	SAMTEC Connector (female)	-	N	5	Y
FFSD-08-D-X.00-01-N	SAMTEC Connector (female)	-	N	1	Y
WM5987-ND	MOLEX Connector (female)	-	N	1	Y
DF13-6S-1.25C	Hirose Connector (female)	-	N	3	Y
DF13-2630SCFA	Hirose Wire Crimp	-	N	18	Y

SMS Circuit Component List (Version 3)

Part Number/Type	Name	Package	Purchase Required?	Quantity	O/H
1 M Ohm	Resistor	Surface Mount 1206	N	2	Y
10k Ohm	Resistor	Surface Mount 1206	N	4	Y
20k Ohm	Resistor	Surface Mount 1206	N	18	Y
100k Ohm	Resistor	Surface Mount 1206	N	2	Y
SMS Ckt 1 X Ohm	Resistor	Surface Mount 1206	N	1	Y
SMS Ckt 2 X Ohm	Resistor	Surface Mount 1206	N	1	Y
10 uF	Capacitor	Surface Mount 3528	N	8	Y
0.01 uF	Capacitor	Surface Mount 0805	N	9	Y
0.1 uF	Capacitor	Surface Mount 0805	N	10	Y
STPS0520Z	Schottky Rectifier	SOD-123	N	6	Y
OP97FSZ	OpAmp	SOIC	N	2	Y
AD620ARZ	Instrument Amp	SOIC	N	2	Y
MAX6633MSA	Temperature Sensor	SOIC	N	1	Y
MAX680ESA+	Voltage Converter	SOIC	N	2	Y
AO4440	MOSFET	SOIC	N	2	Y
MAX4427ESA+	MOSFET Driver	SOIC	N	5	Y
ER422D	Latching Relay	Through Hole	Y	5	Y
WM18926-ND	MOLEX Connector (male)	Through Hole	N	1	Y
FTSH-105-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	5	Y
FTSH-108-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	1	Y
DF13-6P-1.25DSA	Hirose Connector (male)	Through Hole	N	3	Y
VL2320-1F2N	Coin Cell	Surface Mount	N	1	Y
ABS10-32.768KHZ-1-T	Crystal	Surface Mount	N	1	Y
PCA8565TS	Real Time Clock	TSSOP	N	1	Y
SNLVC245APWR	Octal Bus Transceiver	TSSOP	N	1	Y
SN74LVC2G04DBVR	Dual Inverter Gate	SOT-23	N	1	Y
PCA9517DR	I^2C Bus Repeater	SOIC	N	1	Y
SN74LVC126APW	Quadruple Bus Buffer Gate	TSSOP	N	1	Y
ESQ-126-39-G-D	SAMTEC Bus Connector	Through Hole	N	2	Y
SS-411	Two-Axis Digital Sun Sensor	Through Hole	N	1	Y
SMS V3	Printed Circuit Board	N/A	N	1	Y

Connectors:

FFSD-05-D-X.00-01-N	SAMTEC Connector (female)	-	N	5	Y
FFSD-08-D-X.00-01-N	SAMTEC Connector (female)	-	N	1	Y
WM5987-ND	MOLEX Connector (female)	-	N	1	Y
DF13-6S-1.25C	Hirose Connector (female)	-	N	3	Y
DF13-2630SCFA	Hirose Wire Crimp	-	N	18	Y

TOTAL	129

ESP Printed Circuit Board Component List (Version 2)

Part Number/Type	Name	Package	Purchase Required?	Quantity	O/H
0.1 uF	Capacitor	Surface Mount 0805	N	4	Y
MAX6633MSA	Temperature Sensor	SOIC	N	4	Y
FTSH-108-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	1	Y
TASC	Triangular Advanced Solar Cell	Surface Mount	N	2	Y
Silicon	Solar Cell	Surface Mount	N	2	Y

TOTAL	13

Connectors:

FFSD-08-D-X.00-01-N	SAMTEC Connector (female)	-	N	1	Y

ESP Printed Circuit Board Component List (Version 3)

Part Number/Type	Name	Package	Purchase Required?	Quantity	O/H
0.1 uF	Capacitor	Surface Mount 0805	N	4	Y
MAX6633MSA	Temperature Sensor	SOIC	N	4	Y
FTSH-108-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	1	Y
Spectrolab ITJ CIC	Diced Solar Cell	Surface Mount	Y	1	N
Emcore ATJ CIC	Diced Solar Cell	Surface Mount	Y	1	N
Polycrystalline Silicon	Diced Solar Cell	Surface Mount	Y	1	N
Polycrystalline Silicon	Diced Solar Cell	Surface Mount	Y	1	N
			TOTAL	13	
Connectors:					
FFSD-08-D-X.00-01-N	SAMTEC Connector (female)	-	N	1	Y

Solar Panel Printed Circuit Board (Version 1) Component List

Part Number/Type	Name	Package	Purchase Required?	Quantity*	O/H
0.1 uF	Capacitor	Surface Mount 0805	N	10	Y
MAX6633MSA	Temperature Sensor	SOIC	N	10	Y
FTSH-105-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	5	Y
CIC	Cell-Interconnect-Coverglass Solar Cell	Surface Mount	N	8	Y
PA28-2450-120SA (-Z ONLY)	Patch Antenna	Surface Mount	N	1	Y
FTSH-105-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	5	Y
			TOTAL	39	
Connectors:					
FFSD-08-D-X.00-01-N	SAMTEC Connector (female)	-	N	5	Y

*Numbers are for entire satellite including five solar panels (±X,±Y,-Z)

Solar Panel Printed Circuit Board (Version 2) Component List

Part Number/Type	Name	Package	Purchase Required?	Quantity*	O/H
0.1 uF	Capacitor	Surface Mount 0805	N	10	Y
MAX6633MSA	Temperature Sensor	SOIC	N	10	Y
FTSH-108-01-L-D-K	SAMTEC Connector (male)	Through Hole	N	5	Y
CIC (±X/-Y ONLY)	Cell-Interconnect-Coverglass Solar Cell	Surface Mount	N	8	Y
TASC (+Y/-Z ONLY)	Triangular Advanced Solar Cell	Surface Mount	N	16	Y
PA28-2450-120SA (-Z ONLY)	Patch Antenna	Surface Mount	N	1	Y
53047-0410 (+Y ONLY)	MOLEX Connector (male)	Through Hole	N	1	Y
KIT3000UZ (+Y ONLY)	Ceramic RF Capacitor	Surface Mount 0805	Y	1	N
U.FL-R-SMT(01) (+Y ONLY)	Hirose Coaxial Connector (female)	Surface Mount	N	1	Y
ERJ-P08J105V (+Y ONLY)	Resistor	Surface Mount 0805	N	1	Y
AOD444 (+Y ONLY)	N-Channel MOSFET	Surface Mount TO252	N	1	Y
SN74AUC2G241DCUR (+Y ONLY)	IC Buffer Driver	VSSOP	N	1	Y
ERB-S00R50U (+Y ONLY)	Fuse	Surface Mount 0402	N	1	Y
ERB-S00R75U (+Y ONLY)	Fuse	Surface Mount 0402	N	1	Y
ADT1-1WT+ (+Y ONLY)	RF Transformer	Surface Mount	N	1	Y
LFCN-530+ (+Y ONLY)	Low Pass Filter	Surface Mount	N	1	Y
SN74AHCT1G08 (+Y ONLY)	AND Gate	SOT-23	N	1	Y
			TOTAL	58	
Connectors:					
FFSD-05-D-X.00-01-N	SAMTEC Connector (female)	-	N	5	Y
51027-0400 (+Y ONLY)	Molex Connector (female)	-	N	1	Y
50079-8000 (+Y ONLY)	Molex Connector Terminal (female)	-	N	4	Y

*Numbers are for entire satellite including five solar panels (±X,±Y,-Z)

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APPENDIX B: COMPONENT TEMPERATURE LIMITS

BMS Printed Circuit Board (Version 1) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
1 M Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
49.9 Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
10 uF	LOW ESR TPS SERIES CAPACITOR	Capacitor	Surface Mount 6032	-55	-55	125	125
0.01 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
OP97EP	IC OPAMP LOW-POWER OP97	OpAmp	8-PDIP	-65	-40	85	150
AD620BN	IC AMP INSTRUMENTATION	Instrumentation Amp	8-PDIP	-65	-40	85	125
MAX680EPA	IC VOLT CONVERTER	Voltage Converter	8-PDIP	-65	-40	85	160
STPS0520Z	DIODE SCHOTTKY 20V 0.5A	Schottky Rectifier	SOD-123	-65	-65	125	125
2N6798	POWER MOSFET N-CH 8A 100V	MOSFET	TO-205AF	-55	-55	150	150

Connectors:

35507-0800	CONN RECEPTCL HOUSING 8POS 2MM	MOLEX Connector (female)	-	-40	-40	105	105
35362-0850	CONN HEADER 8POS 2MM VERT TIN	MOLEX Connector (male)	Through Hole	-40	-40	105	105

SIBS Printed Circuit Board (Version 2) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
1 M Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
10k Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
20k Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
100k Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
SMS Ckt 1 X Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
SMS Ckt 2 X Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
10 uF	LOW ESR TPS SERIES CAPACITOR	Capacitor	Surface Mount 3528	-55	-55	125	125
0.01 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
STPS0520Z	DIODE SCHOTTKY 20V 0.5A	Schottky Rectifier	SOD-123	-65	-65	125	125
OP97FSZ	IC OPAMP LOW-POWER OP07	OpAmp	8-SOIC	-65	-40	85	150
AD620ARZ	IC AMP INSTRUMENTATION	Instrumentation Amp	8-SOIC	-65	-40	85	150
MAX6633MSA	IC TEMP SENSOR SMBUS	Temperature Sensor	8-SOIC	-65	-55	150	150
MAX680ESA+	IC VOLT CONVERTER	Voltage Converter	8-SOIC	-65	-40	85	160
AO4440	MOSFET N-CH 60V 5A	MOSFET	8-SOIC	-55	-55	150	150
MAX4427ESA+	IC MOSFET DRV DUAL NONINV	MOSFET Driver	8-SOIC	-55	-40	85	160
ER422D	MAGNETIC LATCHING RELAY	Latching Relay	Through Hole	-65	-65	125	125
VL2320-1F2N	BATT LITH COIN 3V 23MM PCB TAB	Coin Cell	Surface Mount	-20	-20	60	60
ABS10-32.768KHZ-1-T	CRYSTAL 32.768KHZ 12.5PF SMD	Crystal	Surface Mount	-55	-40	85	125
PCA8565TS	IC CMOS RTC/CALENDAR	Real Time Clock	8-TSSOP	-40	-40	125	125
SNLVC245APWR	IC BUS TRANSCVR OCTAL	Octal Bus Transceiver	20-TSSOP	-65	-40	85	150
SN74LVC2G04DBVR	IC DUAL INVERTER GATE	Dual Inverter Gate	SOT-23	-65	-40	85	150
PCA9517DR	IC I2C BUS REPEATER	I^2C Bus Repeater	8-SOIC	-65	-40	85	150
SN74LVC126APW	IC BUS BUFF TRI-ST QD	Quadruple Bus Buffer Gate	14-TSSOP	-65	-40	125	150
SS-411	TWO-AXIS DIGITAL SUN SENSOR	Sun Sensor	-	-40	-25	70	85
Connectors:							
35362-0850	CONN HEADER 8POS 2MM VERT TIN	MOLEX Connector (male)	Through Hole	-40	-40	105	105
FTSH-105-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
FTSH-108-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
DF13-6P-1.25DSA	CONN HEADER 6POS 1.25MM STR TIN	Hirose Connector (male)	Through Hole	-10	-35	85	60
FFSD-05-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105
FFSD-08-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105
35507-0800	CONN RECEPTCL HOUSING 8POS 2MM	MOLEX Connector (female)	-	-40	-40	105	105
DF13-6S-1.25C	CONN SOCKET HOUSING 6POS 1.25MM	Hirose Connector (female)	-	-10	-35	85	60
DF13-2630SCFA	CONN CONTACT 26-30AWG CRIMP GOLD	Hirose Wire Crimp	-	-10	-35	85	60

SMS Printed Circuit Board (Version 3) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
1 M Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
10k Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
20k Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
100k Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
SMS Ckt 1 X Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
SMS Ckt 2 X Ohm	PRECISION THICK FILM CHIP RESISTOR	Resistor	Surface Mount 1206	-55	-55	125	125
10 uF	LOW ESR TPS SERIES CAPACITOR	Capacitor	Surface Mount 3528	-55	-55	125	125
0.01 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
STPS0520Z	DIODE SCHOTTKY 20V 0.5A	Schottky Rectifier	SOD-123	-65	-65	125	125
OP97FSZ	IC OPAMP LOW-POWER OP07	OpAmp	8-SOIC	-65	-40	85	150
AD620ARZ	IC AMP INSTRUMENTATION	Instrumentation Amp	8-SOIC	-65	-40	85	150
MAX6633MSA	IC TEMP SENSOR SMBUS	Temperature Sensor	8-SOIC	-65	-55	150	150
MAX680ESA+	IC VOLT CONVERTER	Voltage Converter	8-SOIC	-65	-40	85	160
AO4440	MOSFET N-CH 60V 5A	MOSFET	8-SOIC	-55	-55	150	150
MAX4427ESA+	IC MOSFET DRV DUAL NONINV	MOSFET Driver	8-SOIC	-55	-40	85	160
ER422D	MAGNETIC LATCHING RELAY	Latching Relay	Through Hole	-65	-65	125	125
VL2320-1F2N	BATT LITH COIN 3V 23MM PCB TAB	Coin Cell	Surface Mount	-20	-20	60	60
ABS10-32.768KHZ-1-T	CRYSTAL 32.768KHZ 12.5PF SMD	Crystal	Surface Mount	-55	-40	85	125
PCA8565TS	IC CMOS RTC/CALENDAR	Real Time Clock	8-TSSOP	-40	-40	125	125
SNLVC245APWR	IC BUS TRANSCVR OCTAL	Octal Bus Transceiver	20-TSSOP	-65	-40	85	150
SN74LVC2G04DBVR	IC DUAL INVERTER GATE	Dual Inverter Gate	SOT-23	-65	-40	85	150
PCA9517DR	IC I2C BUS REPEATER	I^2C Bus Repeater	8-SOIC	-65	-40	85	150
SN74LVC126APW	IC BUS BUFF TRI-ST QD	Quadruple Bus Buffer Gate	14-TSSOP	-65	-40	125	150
SS-411	TWO-AXIS DIGITAL SUN SENSOR	Sun Sensor	-	-40	-25	70	85
Connectors:							
35362-0850	CONN HEADER 8POS 2MM VERT TIN	MOLEX Connector (male)	Through Hole	-40	-40	105	105
FTSH-105-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
FTSH-108-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
DF13-6P-1.25DSA	CONN HEADER 6POS 1.25MM STR TIN	Hirose Connector (male)	Through Hole	-10	-35	85	60
FFSD-05-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105
FFSD-08-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105
35507-0800	CONN RECEPTCL HOUSING 8POS 2MM	MOLEX Connector (female)	-	-40	-40	105	105
DF13-6S-1.25C	CONN SOCKET HOUSING 6POS 1.25MM	Hirose Connector (female)	-	-10	-35	85	60
DF13-2630SCFA	CONN CONTACT 28-30AWG CRIMP GOLD	Hirose Wire Crimp	-	-10	-35	85	60

ESP Printed Circuit Board (Version 2) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
MAX6633MSA	IC TEMP SENSOR SMBUS	Temperature Sensor	8-SOIC	-65	-55	150	150
TASC	TRIANGULAR ADVANCED SOLAR CELL	Ultra Triple Junction Solar Cell	Surface Mount				
Silicon	SOLAR CELL	Single Junction Silicon Solar Cell	Surface Mount				
Connectors:							
FTSH-108-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
FFSD-08-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105

ESP Printed Circuit Board (Version 3) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
MAX6633MSA	IC TEMP SENSOR SMBUS	Temperature Sensor	8-SOIC	-65	-55	150	150
Spectrolab ITJ CIC	DICED SOLAR CELL	Ultra Triple Junction Solar Cell	Surface Mount				
Emcore ATJ CIC	DICED SOLAR CELL	Advanced Triple Junction Solar Cell	Surface Mount				
Polycrystalline Silicon	DICED SOLAR CELL	Single Junction Silicon Solar Cell	Surface Mount				
Polycrystalline Silicon	DICED SOLAR CELL	Single Junction Silicon Solar Cell	Surface Mount				
Connectors:							
FTSH-108-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
FFSD-08-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105

Solar Panel Printed Circuit Board (Version 1) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
MAX6633MSA	IC TEMP SENSOR SMBUS	Temperature Sensor	8-SOIC	-65	-55	150	150
TASC	TRIANGULAR ADVANCED SOLAR CELL	Ultra Triple Junction Solar Cell	Surface Mount				
CIC	CELL-INTERCONNECT-COVERGLASS	Improved Triple Junction Solar Cell	Surface Mount				
PA28-245C-120SA (-Z ONLY)	PATCH ANTENNA	Patch Antenna	Surface Mount				
FTSH-105-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
Connectors:							
FFSD-05-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105

Solar Panel Printed Circuit Board (Version 2) Component Temperature Ranges

Component Designation	Component Nomenclature	Component Common Name	Package	Minimum Temperature (°C)		Maximum Temperature (°C)	
				Storage	Operating	Operating	Storage
0.1 uF	MULTILAYER CERAMIC CAPACITOR	Capacitor	Surface Mount 0805	-55	-55	125	125
MAX6633MSA	IC TEMP SENSOR SMBUS	Temperature Sensor	8-SOIC	-65	-55	150	150
TASC (+Y/-Z only)	TRIANGULAR ADVANCED SOLAR CELL	Ultra Triple Junction Solar Cell	Surface Mount				
CIC (±X,-Y only)	CELL-INTERCONNECT-COVERGLASS	Improved Triple Junction Solar Cell	Surface Mount				
CV4-1161-5	CONTROLLED VOLATILITY ADHESIVE TAPE	NuSil Adhesive Tape	Surface Mount				
FTSH-105-01-L-D-K	MICRO TERMINAL	SAMTEC Connector (male)	Through Hole	-55	-55	105	105
Connectors:							
FFSD-05-D-X.00-01-N	DUAL ROW SOCKET, IDC ASSEMBLY	SAMTEC Connector (female)	-	-55	-55	105	105
+Y-AXIS PANEL ONLY							
KIT3000UZ	CAP CERM HI FREQ 0805	Ceramic RF Capacitor	Surface Mount 0805	-55	-55	125	125
ERJ-P08J105V	RES ANTI-SURGE 1M OHM 5%	Resistor	Surface Mount 0805	-55	-55	155	155
AOD444	MOSFET N-CH 60V 12A	N-Channel MOSFET	Surface Mount TO252	-55	-55	175	175
SN74AUC23241DGVR	IC BUFF/DVR TRI-ST DL	IC Buffer Driver	VSSOP	-65	-40	85	150
ERB-SD0R50U	FUSE 0.5A 24V FAST	Fuse	Surface Mount 0402	-40	-40	100	100
ERB-SD0R75U	FUSE 0.75A 24V FAST	Fuse	Surface Mount 0402	-40	-40	100	100
ADT1-1WT+	TRANSFORMER, RF, SURF MOUNT	RF Transformer	Surface Mount	-55	-20	85	100
LFCN-530+	FILTER, LOW PASS, SURF MOUNT	Low Pass Filter	Surface Mount	-55	-55	100	100
SN74AHCT1G08	IC AND GATE	AND Gate	SOT-23	-65	-40	85	150
U.FL-R-SMT(01)	CONN RECPT ULTRA-MINI COAX SMD	Hirose Coaxial Connector (female)	Surface Mount	-40	-40	90	90
53047-0410	CONN HEADER 4POS 1.25MM VERT TIN	Molex Connector (male)	Through Hole	-40	-40	105	105
Connectors:							
51027-0400	CONN HOUSING 4POS 1.25MM	Molex Connector (female)	-	-40	-40	105	105

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APPENDIX C: CIRCUIT BOARD NET LISTS

SMS Circuit Component-Net-Pin List (Version 1)

FB430 Use	FB430 Pin	CubeSat Bus Pin	SMS Circuit Net	Component(s)	Component Connection	Notes
DAC1	P6.7	H2.1	H2.1	SMS Circuits	-	DAC Output to SMS Circuits 1 and 2
ADC2	P6.2	H2.6	H2.6	SMS Circuit 2	-	ADC2 Input from SMS Circuit 2
ADC1	P6.1	H2.7	H2.7	SMS Circuit 1	-	ADC1 Input from SMS Circuit 1
I/O	P2.7	H2.17	H2.17	Sun Sensor	MOSI	Sun Sensor Pin 7 (MOSI), Blue Wire
I/O	P2.6	H2.18	H2.18	Sun Sensor Temp Sensors	MISO SO	Sun Sensor Pin 3 (MISO), Red Wire Temp Sensor Connector Pin 4 (SO), White Wire
I/O	P2.5	H2.19	H2.19	Sun Sensor	/SS	Sun Sensor Pin 2 (/SS), Brown Wire
I/O	P2.4	H2.20	H2.20	Temp Sensors	/CS4	Temp Sensor Connector Pin 8 (CS4), White Wire
I/O	P2.3	H2.21	H2.21	Temp Sensors	/CS3	Temp Sensor Connector Pin 7 (CS3), Red Wire
I/O	P2.2	H2.22	H2.22	Temp Sensors	/CS2	Temp Sensor Connector Pin 6 (CS2), White Wire
I/O	P2.1	H2.23	H2.23	Temp Sensors	/CS1	Temp Sensor Connector Pin 5 (CS1), Red Wire
I/O	P2.0	H2.24	H2.24	Sun Sensor Temp Sensors	SCK SCK	Sun Sensor Pin 8 (SCK), Purple Wire Temp Sensor Connector Pin 3 (SCK), Red Wire
PWR	+5V	H2.25	H2.25	ALL	-	System Power
PWR	+5V	H2.26	H2.25	ALL	-	Connected to H2.25 pin on SMS board
PWR	VCC (+3.3V)	H2.27	H2.27	NONE	-	Not connected
PWR	VCC (+3.3V)	H2.28	H2.28	NONE	-	Not connected
PWR	GND	H2.29	H2.29	ALL	-	System Ground
PWR	GND	H2.30	H2.29	ALL	-	Connected to H2.29 pin on SMS board
PWR	AGND	H2.31	H2.29	ALL	-	Connected to H2.29 pin on SMS board
PWR	GND	H2.32	H2.29	ALL	-	Connected to H2.29 pin on SMS board

SSB Circuit Component-Unit Pin List [Version 2]

FM430 Pin	CubeSat Bus Pin	SSB Circuit Unit	Component(s)	Connection Type/Name	Notes
P6.7	H2.1	H2.1	SSB Circuits	-	GND Output to SSB Circuits 1 and 2
P6.6	H2.9	H2.9	SSB Circuit 2	-	AGND Input from SSB Circuit 2
P6.1	H2.7	H2.7	SSB Circuit 1	-	AGND Input from SSB Circuit 1
P2.7	H2.17	H2.17	FM430 Bus Isolation	MOSI	SPI Master Out Slave In (MOSI) from FM430 to Bus Isolation Chip 128A
-	-	MOSI	Bus Isolation Sun Sensor	MOSI	SPI Master Out Slave In (MOSI) from Bus Isolation Chip 128A to Sun Sensor, Sun Sensor Pin 7, Blue Wire
P2.6	H2.18	H2.18	FM430 Bus Isolation	MISO	SPI Master In Slave Out (MISO) from FM430 to Bus Isolation Chip 128A
-	-	MISO	Bus Isolation Sun Sensor	MISO	SPI Master In Slave Out (MISO) from Bus Isolation Chip 128A to Sun Sensor, Sun Sensor Pin 3, Red Wire
P2.5	H2.24	H2.24	FM430 Bus Isolation	SCK	SPI Serial Clock (SCK) from FM430 to Bus Isolation Chip 128A
-	-	SCK	Bus Isolation Sun Sensor	SCK	SPI Serial Clock (SCK) from Bus Isolation Chip 128A to Sun Sensor, Sun Sensor Pin 8, Purple Wire
P2.3	H2.19	H2.19	FM430 Bus Isolation	ANT	SPI Chip Select (SS) from FM430 to Bus Isolation Chip 128A
-	-	SS	Bus Isolation Sun Sensor	ANT	SPI Chip Select (SS) from Bus Isolation Chip 128A to Sun Sensor, Sun Sensor Pin 2, Brown Wire
P1.1	H2.15	H2.15	FM430 Bus Isolation	SCL	I²C Serial Clock (SCL) Line from Bus Isolation Chip PCA9517 to I2C Temperature Sensors
-	-	SCL	Bus Isolation Temperature Sensors	SCL	I²C Serial Clock (SCL) Line from FM430 to Bus Isolation Chip PCA9517
P1.2	H2.14	H2.14	FM430 Bus Isolation	SDA	I²C Serial Data (SDA) Line from Bus Isolation Chip PCA9517 to I²C Temperature Sensors
-	-	SDA	Bus Isolation Temperature Sensors	SDA	I²C Serial Data (SDA) Line from FM430 to Bus Isolation Chip PCA9517
P4.0	H1.10	H1.10	Bus Isolation	BUS_I2C	TTL signal from FM430 to enable the bus isolation circuitry
P5.0	H1.9	H1.9	FM430 Bus Isolation	R1A	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 1 Coil A to run motor axis to EPS
-	-	RL1RA	Bus Isolation Relay 1 MOSFET Driver	RL1RA	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 1 Coil A to run motor axis to EPS
P5.1	H1.7	H1.7	FM430 Bus Isolation	R1B	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 1 Coil B to run motor axis to SSB
-	-	RL1RB	Bus Isolation Relay 1 MOSFET Driver	RL1RB	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 1 Coil B to run motor axis to SSB
P5.2	H1.8	H1.8	FM430 Bus Isolation	R2A	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 2 Coil A to run motor axis to EPS
-	-	RL2RA	Bus Isolation Relay 2 MOSFET Driver	RL2RA	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 2 Coil A to run motor axis to EPS
P5.3	H1.5	H1.5	FM430 Bus Isolation	R2B	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 2 Coil B to run motor axis to SSB
-	-	RL2RB	Bus Isolation Relay 2 MOSFET Driver	RL2RB	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 2 Coil B to run motor axis to SSB
P5.4	H1.4	H1.4	FM430 Bus Isolation	R3A	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 3 Coil A to run motor axis to EPS
-	-	RL3RA	Bus Isolation Relay 3 MOSFET Driver	RL3RA	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 3 Coil A to run motor axis to EPS
P5.5	H1.3	H1.3	FM430 Bus Isolation	R3B	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 3 Coil B to run motor axis to SSB
-	-	RL3RB	Bus Isolation Relay 3 MOSFET Driver	RL3RB	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 3 Coil B to run motor axis to SSB
P5.6	H1.2	H1.2	FM430 Bus Isolation	R4A	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 4 Coil A to run motor axis to EPS
-	-	RL4RA	Bus Isolation Relay 4 MOSFET Driver	RL4RA	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 4 Coil A to run motor axis to EPS
P5.7	H1.1	H1.1	FM430 Bus Isolation	R4B	Pulsed TTL signal from FM430 to Bus Isolation Chip 245A, used to activate Relay 4 Coil B to run motor axis to SSB
-	-	RL4RB	Bus Isolation Relay 4 MOSFET Driver	RL4RB	Pulsed TTL signal from Bus Isolation Chip 245A to activate Relay 4 Coil B to run motor axis to SSB
P3.4	H1.23	H1.23	FM430 Relay 5 MOSFET Driver	R5A	Pulsed TTL signal from FM430 used to activate Relay 5 Coil A to switch off the SSB +5V
P3.5	H1.18	H1.18	FM430 Relay 5 MOSFET Driver	R5B	Pulsed TTL signal from FM430 used to activate Relay 5 Coil B to switch on the SSB +5V
-	-	-5V	ALL	+5VRTN	SSB PCB +5V bus supplied by Relay 5. Switched Voltage
+5V	H2.26	H2.26	Relay 5	+5V	Switch +5V controlled by Relay 5
+5V	H2.28	H2.26	Relay 5	-	Connected to H2.26 pin on CubeSat 5V Bus
VCC (+3.3V)	H2.27	H2.27	Temperature Sensors Bus Isolation	V$_{CC}$_3V3	Bus isolation, Temperature Sensor, and I²C Bus Voltage
VCC (+3.3V)	H2.29	H2.27	Temperature Sensors Bus Isolation	V$_{CC}$_3V3	Connected to H2.27 pin on CubeSat 3V Bus
GND	H2.30	H2.30	ALL	GND	System Ground
GND	H2.36	H2.30	ALL	GND	Connected to H2.30 pin on SSB board
AGND	H2.8	H2.30	ALL	AGND	Connected to H2.30 pin on SSB board
GND	H2.32	H2.30	ALL	GND	Connected to H2.30 pin on SSB board
-	-	+15V1	SSB Circuit 1	+15V	Positive Steady Voltage for SSB Circuit 1 Components
-	-	-15V1	SSB Circuit 1	-15V	Negative Steady Voltage for SSB Circuit 1 Components
-	-	+15V2	SSB Circuit 2	+15V	Positive Steady Voltage for SSB Circuit 2 Components
-	-	-15V2	SSB Circuit 2	-15V	Negative Steady Voltage for SSB Circuit 2 Components
-	-	SC1+	Experimental Solar Cell 1 Relay 1	SC1	Experimental Solar Cell 1 Positive Lead connected to Relay 1
-	-	SC1-	Experimental Solar Cell 1 Relay 1	SC1	Experimental Solar Cell 1 Negative Lead connected to Relay 1
-	-	SC2+	Experimental Solar Cell 2 Relay 2	SC2	Experimental Solar Cell 2 Positive Lead connected to Relay 2
-	-	SC2-	Experimental Solar Cell 2 Relay 2	SC2	Experimental Solar Cell 2 Negative Lead connected to Relay 2
-	-	SC3+	Experimental Solar Cell 3 Relay 3	SC3	Experimental Solar Cell 3 Positive Lead connected to Relay 3
-	-	SC3-	Experimental Solar Cell 3 Relay 3	SC3	Experimental Solar Cell 3 Negative Lead connected to Relay 3
-	-	SC4+	Experimental Solar Cell 4 Relay 4	SC4	Experimental Solar Cell 4 Positive Lead connected to Relay 4
-	-	SC4-	Experimental Solar Cell 4 Relay 4	SC4	Experimental Solar Cell 4 Negative Lead connected to Relay 4
-	-	+XSC+	+X-Axis Connector EPS Header SA2	-	Positive X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 1, EPS out +X_VARRAY
-	-	+XSC-	+X-Axis Connector EPS Header SA2	-	Positive X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 2, EPS out GND
-	-	-XSC+	-X-Axis Connector EPS Header SA2	-	Negative X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 4, EPS out -X_VARRAY
-	-	-XSC-	-X-Axis Connector EPS Header SA2	-	Negative X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 5, EPS out GND
-	-	+YSC+	+Y-Axis Connector EPS Header SA1	-	Positive Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 1, EPS out +Y_VARRAY
-	-	+YSC-	+Y-Axis Connector EPS Header SA1	-	Positive Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 2, EPS out GND
-	-	-YSC+	-Y-Axis Connector EPS Header SA1	-	Negative Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 4, EPS out -Y_VARRAY
-	-	-YSC-	-Y-Axis Connector EPS Header SA1	-	Negative Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 5, EPS out GND
-	-	+ZSC+	+Z-Axis Connector EPS Header SA3	-	Positive Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 1, EPS out +Z_VARRAY
-	-	+ZSC-	+Z-Axis Connector EPS Header SA3	-	Positive Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 2, EPS out GND
-	-	-ZSC+	-Z-Axis Connector EPS Header SA3	-	Negative Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 4, EPS out -Z_VARRAY
-	-	-ZSC-	-Z-Axis Connector EPS Header SA3	-	Negative Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 5, EPS out GND

SMS Circuit Component-Net-Pin List (Version X)

Identifier	FRK30 Pin	Cuboid Bus Pin	SMS Circuit Net	Component(s)	Connection Type/Name	Notes
ADC1	P2.7	H2.1	H2.1	SMS Circuit	-	ADC Output to SMS Circuits 1 and 2
ADC2	P2.2	H2.6	H2.6	SMS Circuit 2	-	ADC2 Input from SMS Circuit 2
ADC1	P2.1	H2.7	H2.7	SMS Circuit 1	-	ADC1 Input from SMS Circuit 1
MO	P2.7	H2.17	H2.17	FRK30 Bus Isolator	MOSI	SPI Master Out Slave In (MOSI) from FRK30 to Bus Isolator Chip 128A
MO	-	-	MOSI	Bus Isolator Sun Sensor	MOSI	SPI Master Out Slave In (MOSI) from Bus Isolator Chip 128A to Sun Sensor, Sun Sensor Pin 7, Blue Wire
MO	P2.5	H2.18	H2.18	FRK30 Bus Isolator	MISO	SPI Master In Slave Out (MISO) from FRK30 to Bus Isolator Chip 128A
MO	-	-	MISO	Bus Isolator Sun Sensor	MISO	SPI Master In Slave Out (MISO) from Bus Isolator Chip 128A to Sun Sensor, Sun Sensor Pin 3, Red Wire
MO	P2.9	H2.24	H2.24	FRK30 Bus Isolator	SCK	SPI Serial Clock (SCK) from FRK30 to Bus Isolator Chip 128A
MO	-	-	SCK	Bus Isolator Sun Sensor	SCK	SPI Serial Clock (SCK) from Bus Isolator Chip 128A to Sun Sensor, Sun Sensor Pin 8, Purple Wire
MO	P2.8	H2.19	H2.19	FRK30 Bus Isolator	SS	SPI Chip Select (SS) from FRK30 to Bus Isolator Chip 128A
MO	-	-	SS	Bus Isolator Sun Sensor	SS	SPI Chip Select (SS) from Bus Isolator Chip 128A to Sun Sensor, Sun Sensor Pin 2, Brown Wire
MO	P1.1	H2.15	H2.15	FRK30 Bus Isolator	SCL	I²C Serial Clock (SCL) Line from Bus Isolator Chip PCA9517 to I²C Temperature Sensors
MO	-	-	SCL	Bus Isolator Temperature Sensors	SCL	I²C Serial Clock (SCL) Line from FRK30 to Bus Isolator Chip PCA9517
MO	P1.2	H2.14	H2.14	FRK30 Bus Isolator	SDA	I²C Serial Data (SDA) Line from Bus Isolator Chip PCA9517 to I²C Temperature Sensors
MO	-	-	SDA	Bus Isolator Temperature Sensors	SDA	I²C Serial Data (SDA) Line from FRK30 to Bus Isolator Chip PCA9517
MO	P4.0	H1.10	H1.10	Bus Isolator	BUS_ISO	TTL signal from FRK30 to enable the bus isolation circuitry
MO	P3.0	H1.8	H1.8	FRK30 Bus Isolator Relay 1 MOSFET Driver	R1A	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 1 Coil A to run solar cells to EPS
MO	-	-	RL1NA	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 1 Coil A to run solar cells to EPS		
MO	P5.1	H1.7	H1.7	FRK30 Bus Isolator Relay 1 MOSFET Driver	R1B	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 1 Coil B to run solar cells to SMS
MO	-	-	RL1NB	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 1 Coil B to run solar cells to SMS		
MO	P5.2	H1.6	H1.6	FRK30 Bus Isolator Relay 2 MOSFET Driver	R2A	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 2 Coil A to run solar cells to EPS
MO	-	-	RL2NA	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 2 Coil A to run solar cells to EPS		
MO	P5.3	H1.5	H1.5	FRK30 Bus Isolator Relay 2 MOSFET Driver	R2B	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 2 Coil B to run solar cells to SMS
MO	-	-	RL2NB	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 2 Coil B to run solar cells to SMS		
MO	P5.4	H1.4	H1.4	FRK30 Bus Isolator Relay 3 MOSFET Driver	R3A	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 3 Coil A to run solar cells to EPS
MO	-	-	RL3NA	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 3 Coil A to run solar cells to EPS		
MO	P5.5	H1.3	H1.3	FRK30 Bus Isolator Relay 3 MOSFET Driver	R3B	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 3 Coil B to run solar cells to SMS
MO	-	-	RL3NB	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 3 Coil B to run solar cells to SMS		
MO	P5.6	H1.2	H1.2	FRK30 Bus Isolator Relay 4 MOSFET Driver	R4A	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 4 Coil A to run solar cells to EPS
MO	-	-	RL4NA	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 4 Coil A to run solar cells to EPS		
MO	P5.7	H1.1	H1.1	FRK30 Bus Isolator Relay 4 MOSFET Driver	R4B	Pulsed TTL signal from FRK30 to Bus Isolator Chip 245A, used to activate Relay 4 Coil B to run solar cells to SMS
MO	-	-	RL4NB	Pulsed TTL signal from Bus Isolator Chip 245A to activate Relay 4 Coil B to run solar cells to SMS		
MO	P3.4	H1.22	H1.22	FRK30 Relay 5 MOSFET Driver	R5A	Pulsed TTL signal from FRK30 used to activate Relay 5 Coil A to switch off the SMS +5V
MO	P3.5	H1.19	H1.19	FRK30 Relay 5 MOSFET Driver	R5B	Pulsed TTL signal from FRK30 used to activate Relay 5 Coil B to switch on the SMS +5V
PWR	-	-	+5V	ALL	+5VSW	SMS PCB +5V bus supplied by Relay 5, Switched Voltage
PWR	+5V	H2.25	H2.25	Relay 5	+5V	Switch +5V supplied by Relay 5
PWR	+5V	H2.26	H2.26	Relay 5	-	Connected to H2.25 pin on Cuboid to Bus
PWR	VDD (+3.3V)	H2.27	H2.27	Temperature Sensors Bus Isolator	V_{CC}_SNS	Bus Isolator, Temperature Sensor, and I²C Bus Voltage
PWR	VDD (+3.3V)	H2.28	H2.27	Temperature Sensors Bus Isolator	V_{CC}_SNS	Connected to H2.27 pin on Cuboid to Bus
PWR	GND	H2.29	H2.29	ALL	GND	System Ground
PWR	GND	H2.30	H2.29	ALL	GND	Connected to H2.29 pin on SMS board
PWR	AGND	H2.31	H2.29	ALL	AGND	Connected to H2.29 pin on SMS board
PWR	GND	H2.32	H2.29	ALL	GND	Connected to H2.29 pin on SMS board
PWR	-	-	+15V1	SMS Circuit 1	+15V	Positive Supply Voltage for SMS Circuit 1 Components
PWR	-	-	-15V1	SMS Circuit 1	-15V	Negative Supply Voltage for SMS Circuit 1 Components
PWR	-	-	+15V2	SMS Circuit 2	+15V	Positive Supply Voltage for SMS Circuit 2 Components
PWR	-	-	-15V2	SMS Circuit 2	-15V	Negative Supply Voltage for SMS Circuit 2 Components
PWR	-	-	SC1+	Equatorial Solar Cell 1 Relay 1	SC1	Equatorial Solar Cell 1 Positive Lead connected to Relay 1
PWR	-	-	SC1-	Equatorial Solar Cell 1 Relay 1	SC1	Equatorial Solar Cell 1 Negative Lead connected to Relay 1
PWR	-	-	SC2+	Equatorial Solar Cell 2 Relay 2	SC2	Equatorial Solar Cell 2 Positive Lead connected to Relay 2
PWR	-	-	SC2-	Equatorial Solar Cell 2 Relay 2	SC2	Equatorial Solar Cell 2 Negative Lead connected to Relay 2
PWR	-	-	SC3+	Equatorial Solar Cell 3 Relay 3	SC3	Equatorial Solar Cell 3 Positive Lead connected to Relay 3
PWR	-	-	SC3-	Equatorial Solar Cell 3 Relay 3	SC3	Equatorial Solar Cell 3 Negative Lead connected to Relay 3
PWR	-	-	SC4+	Equatorial Solar Cell 4 Relay 4	SC4	Equatorial Solar Cell 4 Positive Lead connected to Relay4
PWR	-	-	SC4-	Equatorial Solar Cell 4 Relay 4	SC4	Equatorial Solar Cell 4 Negative Lead connected to Relay4
PWR	-	-	+XSC+	+X-Axis Connector EPS Header SA2	-	Positive X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 1, EPS net +X_VARRAY
PWR	-	-	+XSC-	+X-Axis Connector EPS Header SA2	-	Positive X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 2, EPS net GND
PWR	-	-	-XSC+	-X-Axis Connector EPS Header SA2	-	Negative X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 4, EPS net -X_VARRAY
PWR	-	-	-XSC-	-X-Axis Connector EPS Header SA2	-	Negative X-Axis Solar Panel Voltage fed to EPS Header SA2 Pin 5, EPS net GND
PWR	-	-	+YSC+	+Y-Axis Connector EPS Header SA1	-	Positive Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 1, EPS net +Y_VARRAY
PWR	-	-	+YSC-	+Y-Axis Connector EPS Header SA1	-	Positive Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 2, EPS net GND
PWR	-	-	-YSC+	-Y-Axis Connector EPS Header SA1	-	Negative Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 4, EPS net -Y_VARRAY
PWR	-	-	-YSC-	-Y-Axis Connector EPS Header SA1	-	Negative Y-Axis Solar Panel Voltage fed to EPS Header SA 1 Pin 5, EPS net GND
PWR	-	-	+ZSC+	+Z-Axis Connector EPS Header SA3	-	Positive Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 1, EPS net +Z_VARRAY
PWR	-	-	+ZSC-	+Z-Axis Connector EPS Header SA3	-	Positive Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 2, EPS net GND
PWR	-	-	-ZSC+	-Z-Axis Connector EPS Header SA3	-	Negative Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 4, EPS net -Z_VARRAY
PWR	-	-	-ZSC-	-Z-Axis Connector EPS Header SA3	-	Negative Z-Axis Solar Panel Voltage fed to EPS Header SA 3 Pin 5, EPS net GND

ESP Printed Circuit Board Component-Net-Pin List (Versions 2 and 3)

Identifier	FM430 Pin	CubeSat Bus Pin	ESP Circuit Net	Component(s)	Connection Type/Name	Notes
I/O	P2.2	H2.22	H2.22	Temperature Sensors	SDA	Temperature Sensor Connector Pin 6 (CS2), White Wire
I/O	P2.1	H2.23	H2.23	Temperature Sensors	SCL	Temperature Sensor Connector Pin 5 (CS1), Red Wire
PWR	VCC (+3.3V)	H2.27	H2.27	Temperature Sensors	V_{CC}_SYS	Temperature Sensor Voltage
PWR	GND	H2.29	H2.29	ALL	GND	System Ground
PWR	-	-	SC1+	Experimental Solar Cell 1	SC1	Experimental Solar Cell 1 Positive Lead connected to SMS PCB
PWR	-	-	SC1-	Experimental Solar Cell 1	SC1	Experimental Solar Cell 1 Negative Lead connected to SMS PCB
PWR	-	-	SC2+	Experimental Solar Cell 2	SC2	Experimental Solar Cell 2 Positive Lead connected to SMS PCB
PWR	-	-	SC2-	Experimental Solar Cell 2	SC2	Experimental Solar Cell 2 Negative Lead connected to SMS PCB
PWR	-	-	SC3+	Experimental Solar Cell 3	SC3	Experimental Solar Cell 3 Positive Lead connected to SMS PCB
PWR	-	-	SC3-	Experimental Solar Cell 3	SC3	Experimental Solar Cell 3 Negative Lead connected to SMS PCB
PWR	-	-	SC4+	Experimental Solar Cell 4	SC4	Experimental Solar Cell 4 Positive Lead connected to SMS PCB
PWR	-	-	SC4-	Experimental Solar Cell 4	SC4	Experimental Solar Cell 4 Negative Lead connected to SMS PCB

APPENDIX D: SOLAR CELL CALCULATIONS

ITJ TASC*				
Jsc	16.9	mA/cm^2	AM0	28°C
Voc	2.565	V		
Area	0.000208	m^2		
Area	2.08	cm^2		
Isc	35.152	mA		
Isc	0.035152	A		
Temp Coeff, Jsc	11.5	uA/cm^2/°C	BOL	
Temp Coeff, Jsc	0.0115	mA/cm^2/°C	BOL	
Temp Coeff, Jsc	12.4	uA/cm^2/°C	EOL	
Temp Coeff, Jsc	0.0124	mA/cm^2/°C	EOL	
Space Temp	1	°C		approximate
Isc, on orbit	35.1635	mA	BOL	
Isc, on orbit	0.035164	A	BOL	
Isc, on orbit	35.1644	mA	EOL	
Isc, on orbit	0.035164	A	EOL	
10% margin	0.03868	A	BOL	
10% margin	0.038681	A	EOL	

UTJ TASC*				
Jsc	17.05	mA/cm^2	AM0	28°C
Voc	2.665	V		
Area	0.000208	m^2		
Area	2.08	cm^2		
Isc	35.464	mA		
Isc	0.035464	A		
Temp Coeff, Jsc	5	uA/cm^2/°C	BOL	
Temp Coeff, Jsc	0.005	mA/cm^2/°C	BOL	
Temp Coeff, Jsc	6	uA/cm^2/°C	EOL	
Temp Coeff, Jsc	0.006	mA/cm^2/°C	EOL	
Space Temp	1	°C		approximate
Isc, on orbit	35.469	mA	BOL	
Isc, on orbit	0.035469	A	BOL	
Isc, on orbit	35.47	mA	EOL	
Isc, on orbit	0.03547	A	EOL	
10% margin	0.0390159	A	BOL	
10% margin	0.039017	A	EOL	

Applied Solar Energy Silicon				
Jsc	36	mA/cm^2	AM1.5	
Voc	0.56	V		
Area	0.000483	m^2		
Area	4.8285	cm^2		
Isc	173.826	mA		
Isc	0.173826	A		
Temp Coeff, Isc	0.00904	mA/K	AM1.5	
Jsc	46	mA/cm^2	AM0	estimation
Isc	222.111	mA		
Isc	0.222111	A		
Space Temp	273	K		approximate
Isc, on orbit	224.5789	mA		
Isc, on orbit	0.224579	A		
10% margin	0.247037	A		

Multicrystalline Silicon Solar Cell Data**			
Area	0.024336	m^2	
Area	243.36	cm^2	
Isc	6.97	A	low
Isc	6970	mA	low
Isc	7.42	A	high
Isc	7420	mA	high
Jsc	286.4069691	A/m^2	low
Jsc	28.64069691	mA/cm^2	low
Jsc	304.8980934	A/m^2	high
Jsc	30.48980934	mA/cm^2	high
Temp Coeff	2.2	mA/K	
Temp Coeff	0.009040105	mA/cm^2/K	

ITJ Experimental Solar Cells				
Jsc	16.9	mA/cm^2	AM0	28°C
Voc	2.565	V		
Area	0.001347	m^2		
Area	13.4663	cm^2		
Isc	227.5805	mA		
Isc	0.22758	A		
Temp Coeff, Jsc	11.5	uA/cm^2/°C	BOL	
Temp Coeff, Jsc	0.0115	mA/cm^2/°C	BOL	
Temp Coeff, Jsc	12.4	uA/cm^2/°C	EOL	
Temp Coeff, Jsc	0.0124	mA/cm^2/°C	EOL	
Space Temp	1	°C		approximate
Isc, on orbit	227.592	mA	BOL	
Isc, on orbit	0.227592	A	BOL	
Isc, on orbit	227.5929	mA	EOL	
Isc, on orbit	0.227593	A	EOL	
10% margin	0.250351	A	BOL	
10% margin	0.250352	A	EOL	

ATJ Experimental Solar Cells[1]				
Jsc	16.9	mA/cm^2	AM0	28°C
Voc	2.575	V		
Area	0.001347	m^2		
Area	13.4663	cm^2		
Isc	227.58047	mA		
Isc	0.22758047	A		
Temp Coeff, Jsc	12	uA/cm^2/°C	BOL	
Temp Coeff, Jsc	0.012	mA/cm^2/°C	BOL	
Temp Coeff, Jsc	12	uA/cm^2/°C	EOL	
Temp Coeff, Jsc	0.012	mA/cm^2/°C	EOL	
Space Temp	1	°C		approximate
Isc, on orbit	227.59247	mA	BOL	
Isc, on orbit	0.22759247	A	BOL	
Isc, on orbit	227.59247	mA	EOL	
Isc, on orbit	0.22759247	A	EOL	
10% margin	0.250351717	A	BOL	
10% margin	0.250351717	A	EOL	

*Ref: Spectrolab
**Ref: HEBE Corporation Photovoltaic Cells
[1]Ref Emcore

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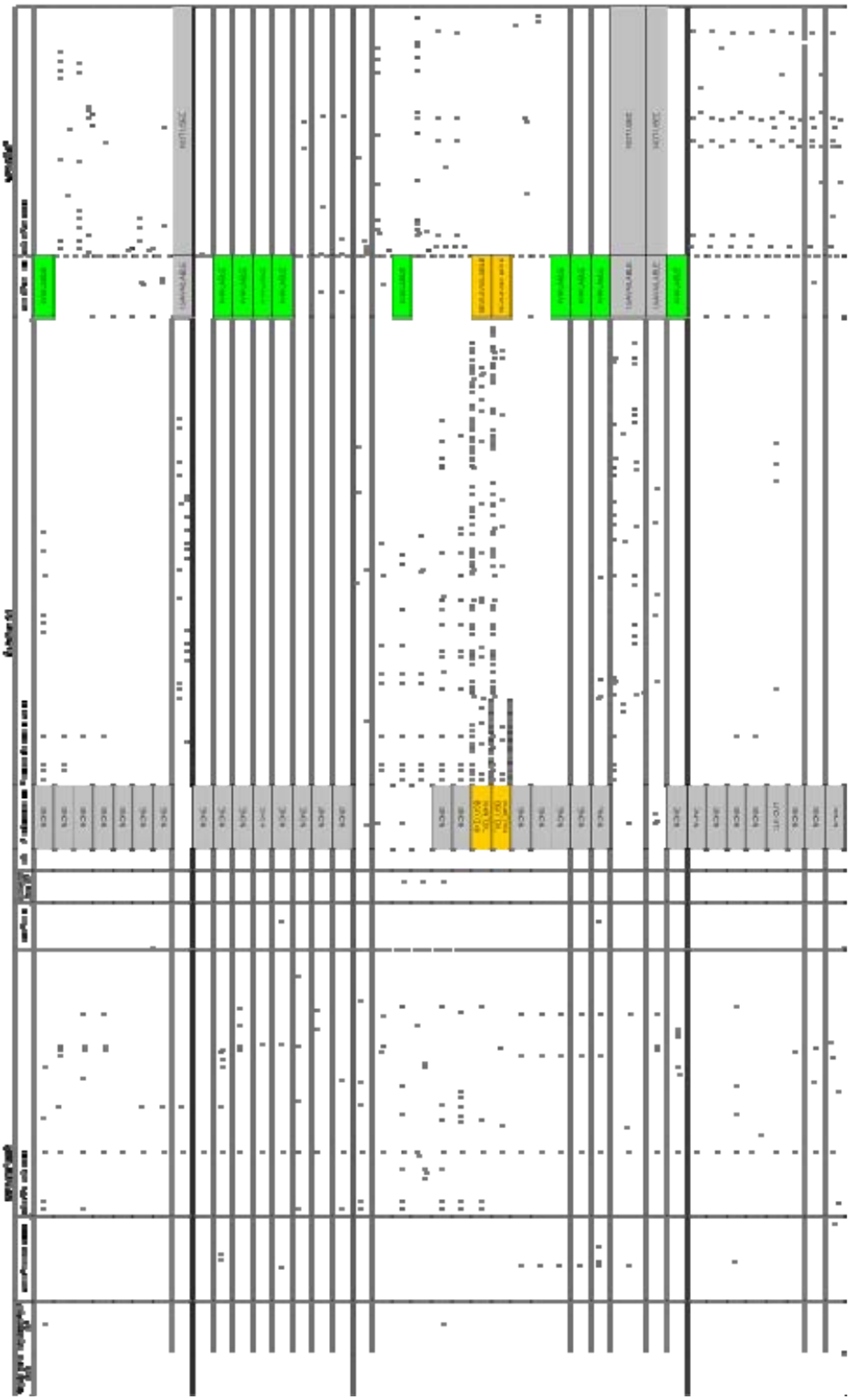
APPENDIX E: FM430 PIN ALLOCATION



88	DV_{SS}	Digital supply voltage, negative terminal. Supplies all digital parts	GND	I/S,SS	PWR		System digital ground			GND		System digital ground
89	DV_{SS}	Digital supply voltage, negative terminal. Supplies all digital parts	GND	I/S,SS	PWR		System digital ground			GND		System digital ground
90	AV_{SS}	Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12	AGND	I/S,SS	PWR		System analog ground. Connected internally to PWR/SS MCU			AGND		System analog ground
91	DV_{SS}	Digital supply voltage, negative terminal. Supplies all digital parts	GND	I/S,SS	PWR		System digital ground			GND		System digital ground
			NO (EEE_MC)	I/S,SS	-		Germane-Ballon-Flight switch normally closed terminal. Battery isolation terminal, connected to battery/Vs - terminal when JP1 is fitted			WHT/ VBAT_CTP_HC		Pull Pin, normally unconnected pin
			NO (EEE_HC)	I/S,SS	-		Germane-Ballon-Flight switch normally closed terminal. Battery isolation terminal, connected to battery/Vs - terminal when JP1 is fitted			WHT/ VBAT_PP_HC		Pull Pin, normally unconnected pin
			S1 (LS_HC)	I/O,SS	-		Lunatic switch normally closed terminal. Battery power disconnect terminal, connected to battery/Vs + terminal right on JP4 is fitted			GRN/ VBAT_SW_HC		Separation flipfob, normally connected pin
			S1 (LS_NC)	I/O,SS	-		Lunatic switch normally closed terminal. Battery power disconnect terminal, connected to battery/Vs + terminal right on JP4 is fitted			GRN/ VBAT_SW_HC		Separation flipfob, normally connected pin
			NO (EEE_MC)	I/S,SS	-		Germane-Ballon-Flight switch normally closed terminal. Battery isolation terminal, connected to battery/Vs + terminal when JP1 is fitted			WHT/ PP_HC		Separate Before Flight switch normally open separation
			NO (EEE_MO)	I/S,SS	-		Germane-Ballon-Flight switch normally open terminal			WHT/ PP_HO		Separate Before Flight switch normally open separation
			S2 (LS_NO)	I/S,SS	-		Lunatic switch normally open terminal			GRN/ SW_HO		Separate Before Flight switch normally open separation
			S2 (LS_NC)	I/O,SS	-		Lunatic switch normally open terminal			GRN/ SW_HO		Separation flipfob, normally connected pin
			S4 (PBF_C)	I/S,IO	-		Remote-Ballon-Flight switch common terminal. Remote ballon terminal, connected to battery/Vs + parallel when JP3 is fitted			WHT/ VBAT_PP_SS_C		Common point for pull pin and separation switch
			S4 (PBF_NC)	I/S,IO	-		Remote-Ballon-Flight switch common terminal. Remote ballon terminal, connected to battery/Vs + parallel when JP3 is fitted			WHT/ VBAT_PP_SS_C		Common point for pull pin and separation switch
			K6 (LS_C)	I/S,IO	-		Lunatic switch normally closed terminal. Battery power disconnect terminal, connected to LDO regulator input terminal when JP4 is fitted			DWG/ VBAT_PP_SS_C		Common point for pull pin and separation switch
			K6 (LS_C)	I/S,IO	-		Lunatic switch normally closed terminal. Battery power disconnect terminal, connected to LDO regulator input terminal when JP4 is fitted			DWG/ VBAT_PP_SS_C		Common point for pull pin and separation switch
			VBATT	I/S,IO	-		Battery voltage, EPS dependent, typically +3V to +8V; connected to battery/+V terminal, can be used to sense voltage prior to battery fuse and diode			BAT_SUB		Output of the battery bus
			VBATT	I/S,IO	-		Battery voltage, EPS dependent, typically +3V to +8V; connected to battery/+V terminal, can be used to sense voltage prior to battery fuse and diode			BAT_SUB		Output of the battery bus
			LVSRW	I/O,nT	I/O		Level-shifted. Not connected to PWB.			RPB_SYNC		Used by Opto Board EPS to synchronize PCM receive enabled power boards. Set inactive as normally timed
			LVSRT	I/S,IO	I/O		Level-shifted. Not connected to PWB.			RPB_SYNC		Used by Opto Board EPS to synchronize PCM receive enabled power boards. Set inactive as normally timed
			LVSCS0	I/S,IO	I/O		Level-shifted. Not connected to PWB.			Not Used		
			LVSCS1	I/S,IO	I/O		Level-shifted. Not connected to PWB.			Not Used		
			LVSCRI	I/S,IO	I/O		Level-shifted. Not connected to PWB.			Not Used		
1	DV_{SS}	Digital supply voltage, positive terminal. Supplies all digital parts. Resistive voltage from onboard LDO, option connects +5V to 3.3V.	-	-	-	-	-	-	-	-	-	-
8	XIN	Input port for crystal oscillator XT1. Can support private crystals can be connected	-	-	-	-	-	-	-	-	-	-
9	XOUT	Output terminal of crystal oscillator XT1	-	-	-	-	-	-	-	-	-	-
62	XT2OUT	Output terminal of crystal oscillator XT2	-	-	-	-	-	-	-	-	-	-
63	XT2IN	Input port for crystal oscillator XT2. Only standard crystals can be connected	-	-	-	-	-	-	-	-	-	-
64	TDO/TDI	Test data output port. TDO/TDI data output or programming data input terminal	-	-	-	-	-	-	-	-	-	-
65	TDI/TCLK	Test data input or test clock input. The device protection fuse is connected to	-	-	-	-	-	-	-	-	-	-
66	TMS	Test mode select. TMS is used as an input port for device programming and test	-	-	-	-	-	-	-	-	-	-
67	TCK	Test clock. TCK is the clock input port for device programming and test operation (scan mode)	-	-	-	-	-	-	-	-	-	-
68	RST/NMI	Reset input, nonmaskable interrupt input port, or boundary (scan mode) pin Flash emulation	-	-	-	-	-	-	-	-	-	-
84	AV_{CC}	Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12. Resistive voltage from onboard LDO, option connects +5V to 3.3V.	-	-	-	-	-	-	-	-	-	-

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APPENDIX F: NPS-SCAT SINGLE NODE THERMAL MODEL

A. MATLAB SCRIPT FILE

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                      NAVAL POSTGRADUATE SCHOOL                              %
%                    SPACE SYSTEMS ACADEMIC GROUP                             %
%                                MONTEREY, CA                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%=========================================================================%
%          NAVAL POSTGRADUATE SCHOOL SOLAR CELL ARRAY TESTER              %
%                        THERMAL CONTROL SUBSYSTEM                        %
%=========================================================================%

%LT Rod Jenkins
%28APR10
%Script file used in conjunction with NPS-SCAT Single Node Thermal
%Model excel spreadsheet.  This file will calculate and produce plots
%of the Sun-orbit angle (Beta) vs. Temperature for NPS-SCAT in both
%the Space Shuttle and Falcon 1e orbits.

clear all;
clc;

%% DEFINE CONSTANTS
%NPS-SCAT
Re=6378.137; %km          EARTH RADIUS
mu=398600.44; %km^3/s^2   EARTH GRAVITATIONAL CONSTANT
sigma=5.67e-8; %W/m^2K^4 BOLTZMANN'S CONSTANT
A=0.06; %m^2              SATELLITE SURFACE AREA
Qeqmax=6.358; %W          EQUIPMENT MAX POWER DISSIPATION (NPS-SCAT EPS)
Qeqmin=0.01; %W           EQUIPMENT MIN POWER DISSIPATION (NPS-SCAT EPS)
Emax=257; %W/m^2  MAX EARTH IR EMISSION AT SURFACE (SMAD, TABLE 11-45A)
Emin=218; %W/m^2  MIN EARTH IR EMISSION AT SURFACE (SMAD, TABLE 11-45A)
S=1367; %W/m^2            DIRECT SOLAR FLUX (SMAD, PP. 432)
a=0.367; %                ALBEDO (NASA EARTH FACT SHEET)
epsilon=0.644; %          EMISSIVITY (BY DESIGN - SEE EXCEL SPREADSHEET)
alpha=0.705; %    ABSORPTIVITY (BY DESIGN - SEE EXCEL SPREADSHEET)
m=0.901517211; %kg        SATELLITE MASS (SEE EXCEL SPREADSHEET)
cp=686.6324818; %J/kg°K   SATELLITE HEAT CAPACITY (SEE EXCEL
SPREADSHEET)
betaD=0; %°               BETA ANGLE

%SPACE STATION ORBIT
hss=336; %km              ORBIT ALTITUDE
iss=51.6461; %°           ORBIT INCLINATION

%FALCON 1E ORBIT
hf1e=450; %km             ORBIT ALTITUDE
if1e=45; %°               ORBIT INCLINATION
```

```
%% SPACE SHUTTLE ORBIT SINGLE NODE THERMAL MODEL CALCULATIONS
%Pre-allocate variables for speed
TssMAX=zeros(181,2);
TssMIN=zeros(181,2);
betass=zeros(181,1);

for betaD=-90:90
    %Sun-Orbit angle
    beta=betaD*(pi/180); %rad
    %Earth angular radius
    rho=asin(Re/(Re+hss)); %rad
    %Orbit Period
    To=(2*pi)/(sqrt(mu))*(Re+hss)^(3/2); %s
    %Eclipse Period
    if((cos(rho)/cos(beta))>1 || (cos(rho)/cos(beta))<-1)
        Te=0; %s
    else
        Te=To*acos(cos(rho)/cos(beta))/pi; %s
    end
    %Sunlight Period
    Ts=To-Te; %s
    %Earth view factor, constant for orbit
    Fe=(1-cos(rho))/2;

    if(Te==0);
        nuMAX=0; %rad
        nuMIN=0; %rad
    elseif(Te~=0)
        nuMAX=acos(cos(rho)/cos(beta)); %rad
        nuMIN=2*pi*Te/To; %rad
    end

    %Diameter of equivalent sphere
    D=sqrt(A/pi); %m
    %Sphere Cross-sectional Area
    Ap=pi*D^2/4; %m^2
    %Solar Environment Input
    Qsolar=Ap*S*alpha; %W
    %Earth Environment Input MAX
    Qearthmax=A*Fe*Emax*epsilon; %W
    %Earth Environment Input MIN
    Qearthmin=A*Fe*Emin*epsilon; %W

    % SHUTTLE ORBIT UPPER TEMPERATURE
    %Albedo view factor
    FaMAX=(Fe*cos(beta)*cos(nuMAX));
    %Maximum Albedo
    QalbedoMAX=A*FaMAX*S*a*alpha; %W
    %Worst Case Hot Temp (without mass)
TmaxMAX=((Qsolar+Qearthmax+QalbedoMAX+Qeqmax)/(sigma*epsilon*A))^(1/4);
%K
    %Worst Case Cold Temp (without mass)
    TminMAX=((Qearthmin+Qeqmin)/(sigma*epsilon*A))^(1/4); %K
    %Mean Temperature
    TavgMAX=((TmaxMAX^4*Ts+TminMAX^4*Te)/To)^(1/4); %K
```

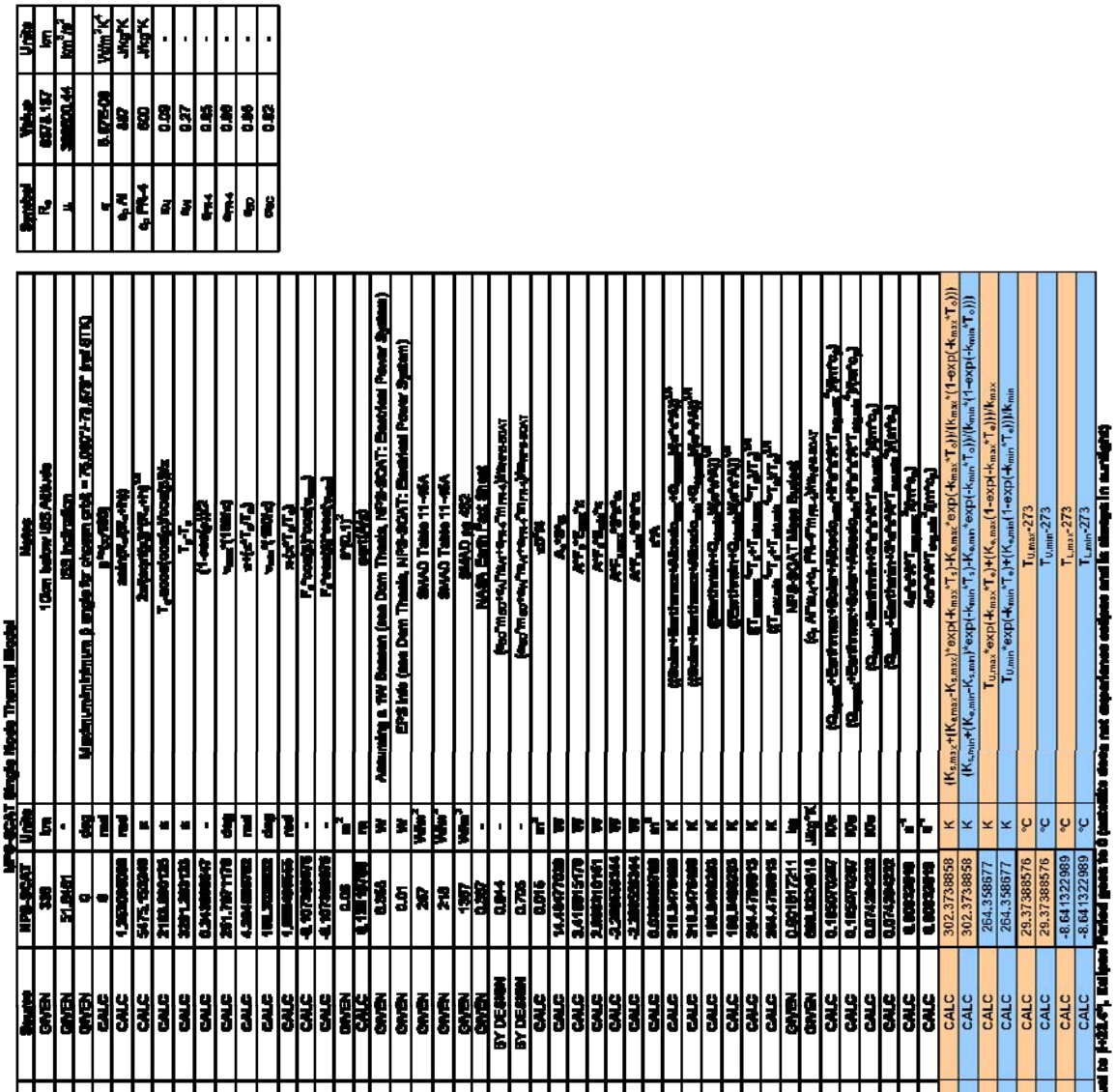
```
    %Sunlight Constant, affected by different nu's
KsMAX=(Qeqmax+Qearthmax+Qsolar+QalbedoMAX+3*sigma*epsilon*A*TavgMAX^4)/
(m*cp); %K/s
    %Eclipse Constant
    KeMAX=(Qeqmin+Qearthmin+3*sigma*epsilon*A*TavgMAX^4)/(m*cp); %K/s
    %Slope
    kMAX=4*sigma*epsilon*A*TavgMAX^3/(m*cp);
    %Upper Temperature (with mass)
    TuMAX=(KsMAX+(KeMAX-KsMAX)*exp(-kMAX*Ts)-KeMAX*exp(-
kMAX*To))/(kMAX*(1-exp(-kMAX*To))); %K
    %Lower Temperature (with mass)
    TlMAX=TuMAX*exp(-kMAX*Te)+(KeMAX*(1-exp(-kMAX*Te)))/kMAX; %K

    TuMAXC=TuMAX-273; %°C
    TlMAXC=TlMAX-273; %°C

    % SHUTTLE ORBIT LOWER TEMPERATURE
    %Albedo view factor
    FaMIN=(Fe*cos(beta)*cos(nuMIN));
    %Minimum Albedo
    QalbedoMIN=A*FaMIN*S*a*alpha; %W
    %Worst Case Hot Temp (without mass)
TmaxMIN=((Qsolar+Qearthmax+QalbedoMIN+Qeqmax)/(sigma*epsilon*A))^(1/4);
%K
    %Worst Case Cold Temp (without mass)
    TminMIN=((Qearthmin+Qeqmin)/(sigma*epsilon*A))^(1/4); %K
    %Mean Temperature
    TavgMIN=((TmaxMIN^4*Ts+TminMIN^4*Te)/To)^(1/4); %K
    %Sunlight Constant
KsMIN=(Qeqmax+Qearthmax+Qsolar+QalbedoMIN+3*sigma*epsilon*A*TavgMIN^4)/
(m*cp); %K/s
    %Eclipse Constant
    KeMIN=(Qeqmin+Qearthmin+3*sigma*epsilon*A*TavgMIN^4)/(m*cp); %K/s
    %Slope
    kMIN=4*sigma*epsilon*A*TavgMIN^3/(m*cp);
    %Upper Temperature (with mass)
    TuMIN=(KsMIN+(KeMIN-KsMIN)*exp(-kMIN*Ts)-KeMIN*exp(-
kMIN*To))/(kMIN*(1-exp(-kMIN*To))); %K
    %Lower Temperature (with mass)
    TlMIN=TuMIN*exp(-kMIN*Te)+(KeMIN*(1-exp(-kMIN*Te)))/kMIN; %K

    TuMINC=TuMIN-273; %°C
    TlMINC=TlMIN-273; %°C

    betass(betaD+91)=betaD;

    TssMAX(betaD+91,1)=TuMAXC;
    TssMAX(betaD+91,2)=TlMAXC;

    TssMIN(betaD+91,1)=TuMINC;
    TssMIN(betaD+91,2)=TlMINC;
end

figure(1);
```

```
plot(betass(:,1),TssMAX(:,1),'r','LineWidth',2);
hold on;
plot(betass(:,1),TssMIN(:,2),'--b','LineWidth',2);
plot([75.060,75.060],[-30,70],'g','LineWidth',2);
plot([-73.679,-73.679],[-30,70],'g','LineWidth',2);
hold off;
grid on;
xlabel('Sun Orbit Angle, \beta, (°)');
ylabel('Temperature (°C)');
xlim([-90,90]);
ylim([-20,65]);
title(['NPS-SCAT Single Node Thermal Model, ',num2str(hss),'km
Altitude, \beta vs. Temperature']);
legend('Upper Temperature','Lower Temperature','Maximum
\beta','Location','Best');


%% FALCON 1E ORBIT SINGLE NODE THERMAL MODEL CALCULATIONS
%Pre-allocate variables for speed
Tf1eMAX=zeros(181,2);
Tf1eMIN=zeros(181,2);
betaf1e=zeros(181,1);

for betaD=-90:90
    %Sun-Orbit angle
    beta=betaD*(pi/180); %rad
    %Earth angular radius
    rho=asin(Re/(Re+hf1e)); %rad
    %Orbit Period
    To=(2*pi)/(sqrt(mu))*(Re+hf1e)^(3/2); %s
    %Eclipse Period
    if((cos(rho)/cos(beta))>1 ||(cos(rho)/cos(beta))<-1)
        Te=0; %s
    else
        Te=To*acos(cos(rho)/cos(beta))/pi; %s
    end
    %Sunlight Period
    Ts=To-Te; %s
    %Earth view factor, constant for orbit
    Fe=(1-cos(rho))/2;

    if(Te==0);
        nuMAX=0; %rad
        nuMIN=0; %rad
    elseif(Te~=0)
        nuMAX=acos(cos(rho)/cos(beta)); %rad
        nuMIN=2*pi*Te/To; %rad
    end

    %Diameter of equivalent sphere
    D=sqrt(A/pi); %m
    %Sphere Cross-sectional Area
    Ap=pi*D^2/4; %m^2
    %Solar Environment Input
```

```
    Qsolar=Ap*S*alpha; %W
    %Earth Environment Input MAX
    Qearthmax=A*Fe*Emax*epsilon; %W
    %Earth Environment Input MIN
    Qearthmin=A*Fe*Emin*epsilon; %W

    % FALCON 1E ORBIT UPPER TEMPERATURE
    %Albedo view factor
    FaMAX=(Fe*cos(beta)*cos(nuMAX));
    %Maximum Albedo
    QalbedoMAX=A*FaMAX*S*a*alpha; %W
    %Worst Case Hot Temp (without mass)
TmaxMAX=((Qsolar+Qearthmax+QalbedoMAX+Qeqmax)/(sigma*epsilon*A))^(1/4);
%K
    %Worst Case Cold Temp (without mass)
    TminMAX=((Qearthmin+Qeqmin)/(sigma*epsilon*A))^(1/4); %K
    %Mean Temperature
    TavgMAX=((TmaxMAX^4*Ts+TminMAX^4*Te)/To)^(1/4); %K
    %Sunlight Constant, affected by different nu's
KsMAX=(Qeqmax+Qearthmax+Qsolar+QalbedoMAX+3*sigma*epsilon*A*TavgMAX^4)/
(m*cp); %K/s
    %Eclipse Constant
    KeMAX=(Qeqmin+Qearthmin+3*sigma*epsilon*A*TavgMAX^4)/(m*cp); %K/s
    %Slope
    kMAX=4*sigma*epsilon*A*TavgMAX^3/(m*cp);
    %Upper Temperature (with mass)
    TuMAX=(KsMAX+(KeMAX-KsMAX)*exp(-kMAX*Ts)-KeMAX*exp(-
kMAX*To))/(kMAX*(1-exp(-kMAX*To))); %K
    %Lower Temperature (with mass)
    TlMAX=TuMAX*exp(-kMAX*Te)+(KeMAX*(1-exp(-kMAX*Te)))/kMAX; %K

    TuMAXC=TuMAX-273; %°C
    TlMAXC=TlMAX-273; %°C

    % FALCON 1E ORBIT LOWER TEMPERATURE
    %Albedo view factor
    FaMIN=(Fe*cos(beta)*cos(nuMIN));
    %Minimum Albedo
    QalbedoMIN=A*FaMIN*S*a*alpha; %W
    %Worst Case Hot Temp (without mass)
TmaxMIN=((Qsolar+Qearthmax+QalbedoMIN+Qeqmax)/(sigma*epsilon*A))^(1/4);
%K
    %Worst Case Cold Temp (without mass)
    TminMIN=((Qearthmin+Qeqmin)/(sigma*epsilon*A))^(1/4); %K
    %Mean Temperature
    TavgMIN=((TmaxMIN^4*Ts+TminMIN^4*Te)/To)^(1/4); %K
    %Sunlight Constant
KsMIN=(Qeqmax+Qearthmax+Qsolar+QalbedoMIN+3*sigma*epsilon*A*TavgMIN^4)/
(m*cp); %K/s
    %Eclipse Constant
    KeMIN=(Qeqmin+Qearthmin+3*sigma*epsilon*A*TavgMIN^4)/(m*cp); %K/s
    %Slope
    kMIN=4*sigma*epsilon*A*TavgMIN^3/(m*cp);
    %Upper Temperature (with mass)
```

```
    TuMIN=(KsMIN+(KeMIN-KsMIN)*exp(-kMIN*Ts)-KeMIN*exp(-
kMIN*To))/(kMIN*(1-exp(-kMIN*To))); %K
    %Lower Temperature (with mass)
    TlMIN=TuMIN*exp(-kMIN*Te)+(KeMIN*(1-exp(-kMIN*Te)))/kMIN; %K

    TuMINC=TuMIN-273; %°C
    TlMINC=TlMIN-273; %°C

    betaf1e(betaD+91)=betaD;

    Tf1eMAX(betaD+91,1)=TuMAXC;
    Tf1eMAX(betaD+91,2)=TlMAXC;

    Tf1eMIN(betaD+91,1)=TuMINC;
    Tf1eMIN(betaD+91,2)=TlMINC;
end

figure(2);
plot(betaf1e(:,1),Tf1eMAX(:,1),'r','LineWidth',2);
hold on;
plot(betaf1e(:,1),Tf1eMIN(:,2),'--b','LineWidth',2);
plot([66.44,66.44],[-30,70],'g','LineWidth',2);
plot([-67.12,-67.12],[-30,70],'g','LineWidth',2);
hold off;
grid on;
xlabel('Sun Orbit Angle, \beta, (°)');
ylabel('Temperature (°C)');
xlim([-90,90]);
ylim([-20,65]);
title(['NPS-SCAT Single Node Thermal Model, ',num2str(hf1e),'km
Altitude, \beta vs. Temperature']);
legend('Upper Temperature','Lower Temperature','Maximum
\beta','Location','Best');
```

B. EXCEL FILE



Symbol	Value	Units
R_e	6371.167	km
μ	398600.44	km^3/s^2
σ	5.67E-08	W/m^2K^4
c_p Air	0.67	J/kg*K
c_p PN-4	800	J/kg*K
η_d	0.59	-
η_e	0.27	-
η_{PN-4}	0.85	-
η_{PD}	0.90	-
η_{SC}	0.92	-

NPS-SCAT CubeSat Mass Budget

	Units	Part	Part Number	Mass / unit	Total Item Mass		Weighed
STRUCTURE	1	Structure Side Walls	Pumpkin 703-00289	63g	63	g	x
	2	Solar Panel Clips (4)	Pumpkin 711-00346	4g	8	g	x
	1	Base Plate Assembly	Pumpkin 703-00294	50g	50	g	x
	1	Cover Plate	Pumpkin 703-00296	31g	31	g	x
	1	Chassis Screws (4) (TOP)	Pumpkin 622-00261	0.5g	2	g	x
	1	Chassis Screws (6) (BOTTOM)	Pumpkin 622-00261	0.5g	3	g	x
	4	Assembly Rods	Pumpkin	1.5g	6	g	x
SUBSYSTEMS	1	+z Solar Panel	Custom	28g	28	g	x
	1	+y Solar Panel	Custom	33.5g	33.5	g	x
	1	+x Solar Panel	Custom	31g	31	g	x
	1	-x Solar Panel	Custom	34g	34	g	x
	1	-y Solar Panel	Custom	34g	34	g	x
	1	-z Solar Panel	Custom	19g	19	g	x
	1	Solar Panel Harness	Samtec	9g	9	g	x
	1	SMS Board + Sun Sensor	Custom	95g	95	g	x
	1	EPS Board	Clyde Space	83g	83	g	x
	1	One Two Cell 10Whr Battery Board	Clyde Space	65g	65	g	x
	1	FM430	710-00252	74g	74	g	x
	1	MHX-2400	Microhard	66g	66	g	x
	1	Beacon	Cal Poly	50g	50	g	
	1	Patch Antenna	Spectrum Controls	17g	17	g	x
		wiring (estimate 5%)	-	5%*1333g	66.65	g	
		thermal (estimate 5%)	-	5%*1333g	66.65	g	

Initial Mass Estimate =	934.817211	g	
Margin =	398.182789	g	29.87%
Total Mass Estimate =	1333	g	

Aluminum Mass=	0.263 kg
FR-4 (PCB) Mass=	0.6385 kg
Solar Cell Mass=	0.017211012 kg

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